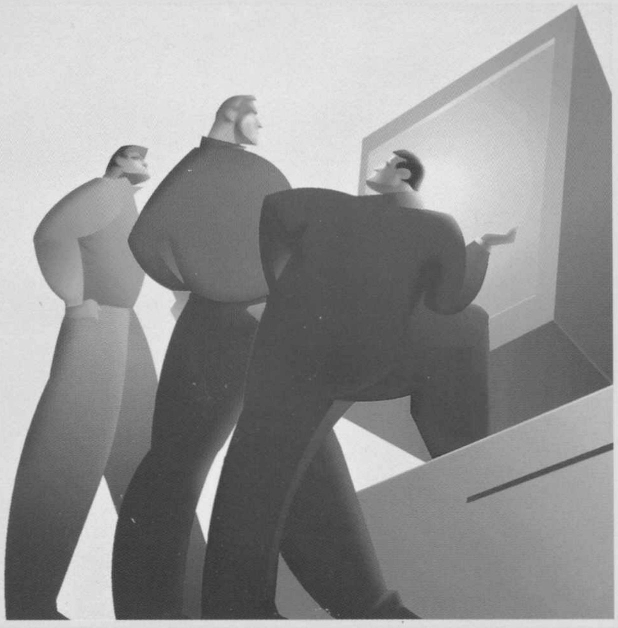
1999 Analog Seminar

Let's Talk Solutions...



From Engineer to Engineer

National Semiconductor

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THE AGE OF INFORMATION STARTS WITH ANALOG SOLUTIONS

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ANALOG SOLUTIONS FOR AMPLIFICATION

Amplifiers

- ➨ *Tiny*
- ➨ *Low Power/Low Voltage*
- ➨ *Precision*
- ➨ *High Speed*

"The Die is the package"

National Analog Solution to the

P.C.Board Crowding Problem

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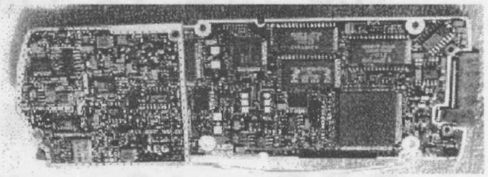
Efficient Use of Board Space

The future of pagers, cellular phones, PDAs and portable electronics:

* Smaller
* Lighter
* Cheaper



Issue: - board space shrinking

- functionality increasing

Solution: Smaller ICs footprint

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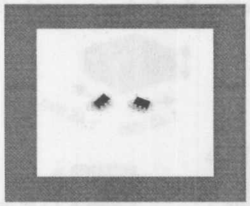
Pagers, Cellular Phones, and PDA's are small portion of a growing list of portable applications where space is a critical issue. Worldwide designers of portable electronics are scrambling for board space.

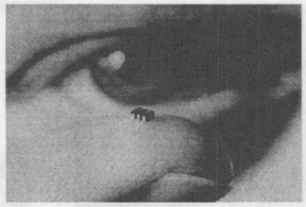
From computers to cell phones, electronics are getting smaller, lighter and cheaper. This is only possible because high levels of integration are reducing the number of components and packages on the circuit boards. The next step is to reduce the size of these packages. National's analog division has introduced new package technologies to meet the demand for efficient use of board space.

National Analog Package Miniaturization Road Map



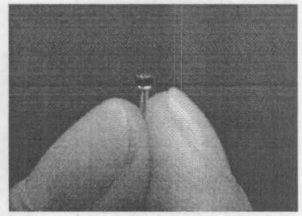
June, 1994 National introduces the first op-amp in the ***SOT23-5 pkg.***

LMC7101



March, 1998 National introduces the World's Smallest op-amp ***in SC70-5 pkg.***

LMV321/821



Sept, 1998 National introduces the World's smallest Dual op-amp, in ***microSMD pkg.***

LMC6035

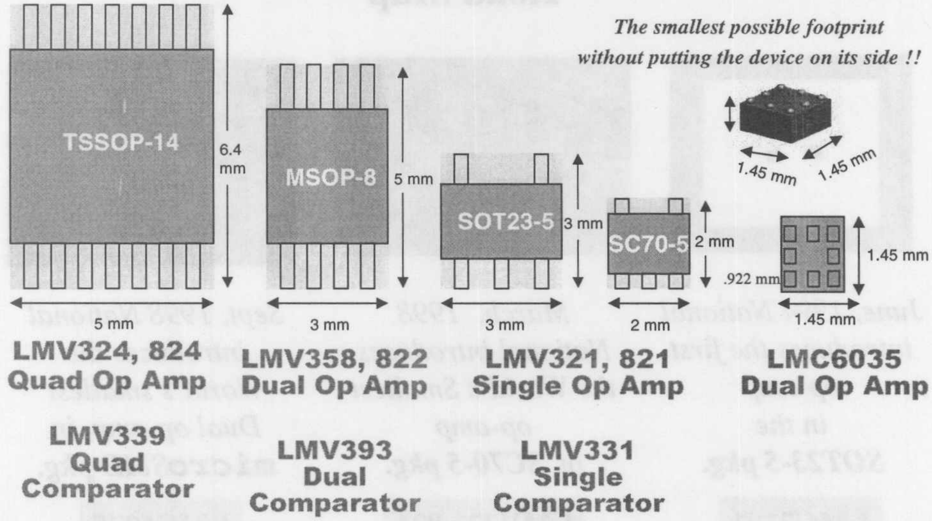
National is a leader in package miniaturization. In June of 1994, National was the first to introduce an op-amp in a 5 lead SOT; the LMC7101.

In March of 1998, National introduced the first op-amp in a 5 lead SC70 package. The SC70 package is a popular discrete transistor package. National engineers have recently designed a series of op-amps capable of fitting into this miniature package. Consequently in March, 1998 National became the first to offer op-amps in the SC-70 package, with the introduction of the LMV321 and the LMV821.

Six months after the introduction of the smallest op-amp, National introduced the world's smallest dual op-amp, the LMC6035 in a microSMD package (Micro Surface Mount Device). The LMC6035 was first introduced in MSOP package about a year ago, and this CMOS dual Op Amp is now offered in a flea-sized package that fits on the head of a pin; the microSMD.

The small footprint of the microSMD package means that system designers can improve system performance by adding more functions in the same board size.

Footprint Comparison



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Above is a footprint comparison of several surface mount I.C. packages offered by National. In the past dual op-amps were offered only in 8-lead SOIC or in 8-lead MSOP. The MSOP package dimensions are (5 X 3) mm^2. The microSMD package is only (1.45 X 1.45) mm^2, or 14% of the MSOP footprint, equivalent to an 86% savings in pc board real estate. In fact the LMC6035 microSMD package footprint is also 50% smaller than the footprint of the single op-amp in the SC70-5 package. Unlike the conventional flip chip package, the microSMD package can be placed on a board using standard SMT placement equipment. Also the microSMD is shipped in the standard tape and reel configuration.

Released Analog Products Per Package Type

TSSOP-14	MSOP-8	SOT23-6	SOT23-5	SC70-5	microSMD	Product Type
LMV324 LMV824	LMV358 LMC272 LMC6482 LMC6572 CLC420 LMC6035		CLC450 LMV321 LMV821 LMC7111 LMC7225 LMC7101	LMV321 LMV821	LMC6035	Op-amp
LMV339	LMV393		LMV331	LMV331		Comparator
	ADC08831 ADC08832	ADCV0831				A/D
	LMC555				LMC555	TIMER
		LM2664 LM2665 LM2681				Switched Cap

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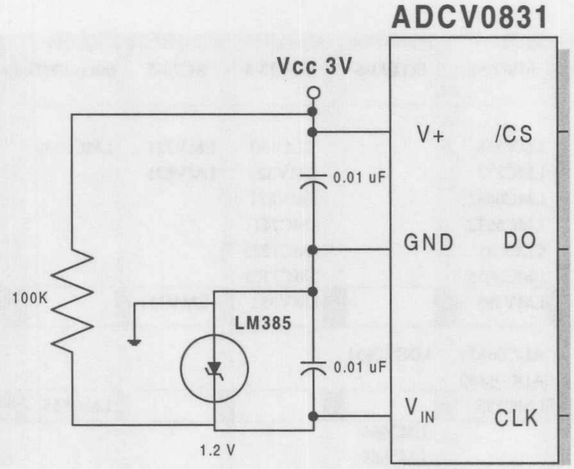
Listed here are some of the National Analog products that are available in small packages types. For a more complete list, be sure to visit the National web site at **www.national.com.**

Power Supply Level Detection



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To demonstrate the combination of versatility and small physical size that can be achieved with these packages, take a look at this power supply voltage level monitor which uses the LM385 and the ADCV0831, both available in a SOT package.

When the supply voltage is at 3V, an LSB for an 8 bit converter is 3/256=11.7 mV. Since the reference voltage is set to 1.2V at the input of the ADCV0831, the output code of the ADCV0831 is therefore 102, representing the 3V supply. As the supply voltage decreases, the LSB decreases and the output code increases. When the supply voltage reaches 2.7V, an LSB is now 10.5mV. Since the converter input voltage input voltage is still 1.2V, and the output code is now 114, representing the 2.7V supply. If the supply voltage increases, the size of the LSB increases and the output code correspondingly decreases. When the supply voltage reaches 3.3V, an LSB is 12.9 mV and the output code is 93.

This application makes an ideal battery monitor for PDAs, handheld phones and portable application. Both the ADCV0831 and LM385 are available in SOT package, to meet the system board space constraints.

ADCV0831	LM385
•First A/D in SOT23-6	• First Reference in a SOT-23
•3V Single Supply Voltage	•1.2V, 2% reference
•8-bit ADC Serial I/O	•8 uA supply current (typ)
•Auto shut down feature	
•Optimized for low power consumption (1mW)	

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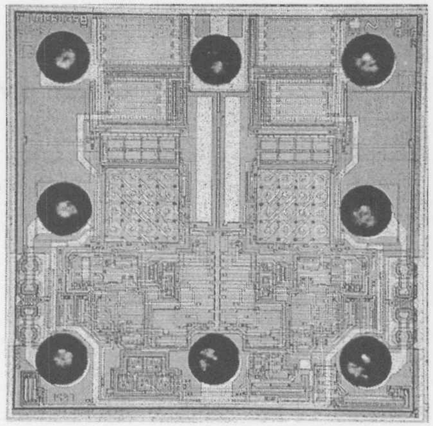
The ADCV0831 is an ideal candidate for 3V applications. Low operating voltage and an auto shutdown feature makes it very suitable for portable battery operated electronic devices.

Not only is the ADCV0831characterised for 3Volt operation, it is the first ADC in a 6 lead SOT package. It is an 8-bit serial I/O device. The LM385 1.2V reference is the first reference in a SOT package.

Actual Photograph of the Top of the LMC6035 Die

1.45 mm



Total Area = 2.10 mm^2

1.45 mm

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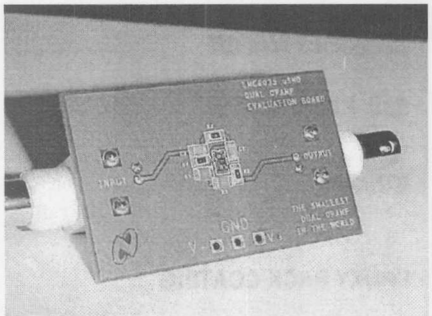
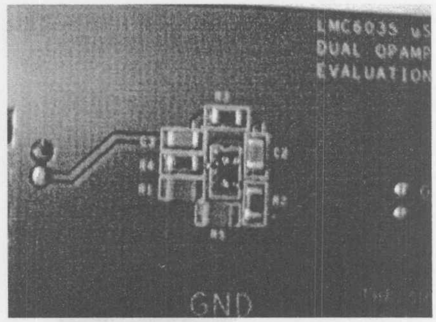
This is a die photo of the LMC6035. The total area of the die (package) is 2.10 mm^2. The die photo shows the 8 bumps placed on respective bond pads. The bumps on the die are 0.5mm pitch, and the bump height is controlled to +/- 15u.

The practical dimensions of the LMC6035 microSMD are identical with the die size shown above.

LMC6035 Evaluation Board





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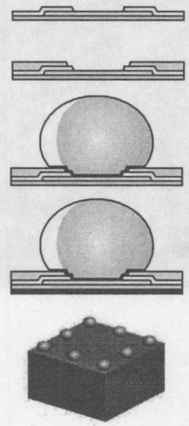
The microSMD package is smaller than a discrete 1210 surface mount resistor. The evaluation board circuit above is a 300 Hz High-pass Active Filter.The board has the microSMD package mounted inside the SOIC outline, to further emphasize the size difference.

microSMD Assembly Flow



- INCOMING WAFER
- 2nd PASSIVATION
- BUMPING
- EPOXY BACK COATING
- SINGULATION

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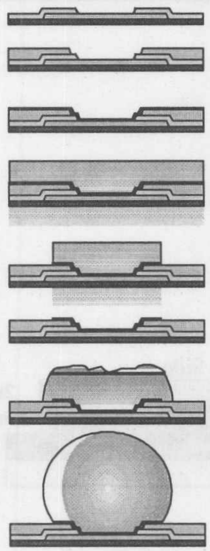
The microSMD assembly process is very simple compared to standard package assembly (i.e SOIC or MSOP). The major processing steps for the microSMD die are the same as for a standard wafer, including implants, metalization, and passivation. However, instead of the wafer processing steps of dice, bond, packaging, and final test, the microSMD assembly process includes a second layer of passivation to protect the die surface followed by the growing of bumps on the bonding pads. The process is complete by placing an epoxy coating on the back of the wafer, final sort, and singulation of the wafer.

The side of the packaging opposite the active geometry side is protected with a proprietary encapsulation. An epoxy back coating is coated on the back of the wafer, this is done for both protection and marking.

Wafer Level Bumping Process Flow



- INCOMING WAFER
- 2nd PASSIVATION
- UBM SPUTTER
- RESIST APPLY
- DEVELOP
- ETCH UBM
- RESIST STRIP
- SOLDER PASTE DEPOSITION
- REFLOW
- CLEAN

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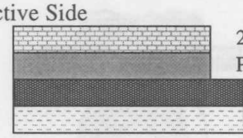
This a more detailed slide of the process. A second passivation is applied to the existing passivation . The second passivation acts as a mechanical stress buffer helping to absorb stress between the solder bumps and metalization of the die.

UBM (Under Bump Metalization) is applied to the wafer. With a photo resist process, UBM is etched from the wafer with the exception of the pad openings. This UBM allows for a solid contact between the bump and die metal.

Solder paste (eutectic Tin/Lead) is then deposited and reflowed. Because of the round shape of UBM pattern, the surface tension of the solder paste causes the bumps to be spherical. The 2nd passivation layer is a non-wettable surface. Therefore, after reflow the solder paste attaches only to the UBM and not to second layer passivation.

Process Summary

- **Top Coat**
- **Bumps**
- **Reflow**
- **Epoxy Backcoat**
- **Mark**
- **Test**
- **Saw**



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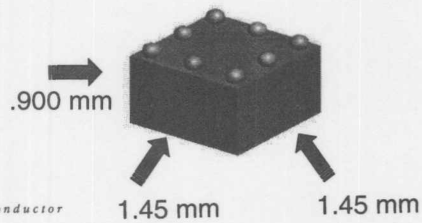
Even thought the microSMD is a "packageless", it still has the necessary markings to identify the products and identify where pin 1 is. The marking is done on the epoxy coating. This back coating also prevents silicon chipping during the saw process. The inert silicon on the edges of the dice protects the active area of the die.

microSMD Package Characterization

•Thermal performance	θ_{JA} =220º C/W, 0 air flow
•Moisture sensitivity	*level 1*
•Package weights	*0.004 gm*
•Package Size	*1.40 mm to 1.45 mm*
•Package Height	*0.90 mm (includes bumps)*



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The microSMD package θ_{JA} is 220 ° C/W which is less than the θ_{JA} of the SC70-5 and SOT23-5. The microSMD package is classified as level 1 for moisture sensitivity. It does NOT require bake and vacuum pack. In the past, several of the surface mount devices such as PQFPs and large PLCC were designated as level 2 moisture sensitivity, which requires special handling, baking and vacuum packing. Furthermore, the microSMD passed all the standard package qualification to 1000 hours.

The LMC6035 microSMD is the smallest possible footprint for an 8-lead package without putting the device on its side. In addition to being the smallest footprint, the height is only 0.9 mm including bumps. This is valuable for applications where the height is critical such as in disk head drives, flat panel displays, cellular phones and PCMCIA cards. Because of the small size shorter interconnections can be made with the advantage of consequently lower inductance and minimal signal degradation in the application.

microSMD package Attributes

- **Smallest** possible footprint per pin.
- No new equipment or handling required.
- Uses standard surface mount techniques
- No need for underfill
- Self-alignment (centering characteristics) during reflow

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microSMD extends the flip chip packaging technology to standard mount technology.

Standard IR eutectic reflow techniques are used to attach the self-aligning bumps, with an added benefit of the microSMD in that underfill is not required. This further simplifies the assembly process, reducing cost and making it possible to rework the board.

The microSMD is shipped in standard polycarbonate carrier tape with pressure sensitive adhesive (PSA) cover tape, and the microSMD technology complies with JEDEC standard MO-211.

National Analog offering of Industry Standard Products in microSMD

Available	•LMC6035	Dual CMOS Op-Amp
	•LMC555	CMOS timer
	•LM431	Precision Reference
	•LM20	Temp sensor
In development	•LM358	Dual Bipolar Op-Amp
	•LM393	Dual Comparator
	•LM2931	Low-Drop out Regulator
	•LM317L	Positive Voltage Regulator
Planned	•LM78L05	Positive Voltage Regulator

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This a list of National Semiconductor releases, present and future, of industry standard products in microSMD package. Offered products will include op-amps, regulators, comparators, references, timers and temp sensors.

Products are being continually selected to meet customers need in their portable systems, and to offer the benefit of smaller footprint to buyers of our industry standard analog I.C.s.

Summary

- LMC6035 in microSMD is the smallest dual op-amp in the world, with twice the functionality, half the size.
- The microSMD package is the cost effective packaging solution
- The microSMD package represents a sea-change in packaging miniaturization for Analog I.C.s. National pioneered this technology.
- microSMD " The Die is the Package."

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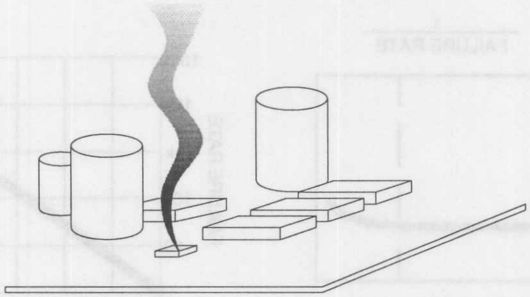
microSMD is a true chipscale package that offers the smallest footprint along with high package robustness, and excellent assembly yield.

microSMD is the most cost - effective package miniaturization solution for portable and handheld products.

Small Package Temperature Ratings



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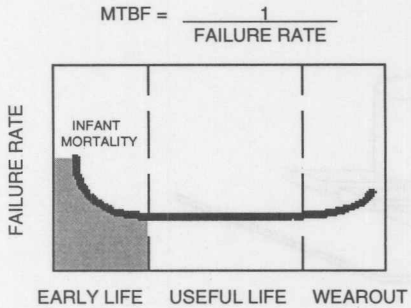
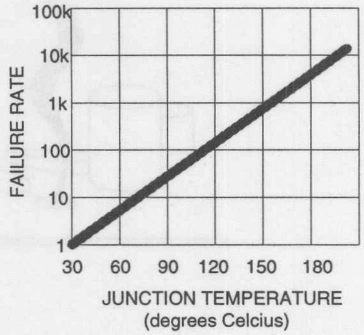
Chip scale packaging clearly offers significant advantages over conventional packages as equipment is increasingly miniaturised or more functionality is crammed into the same enclosure. But, as many have found out, higher density often results in higher operating temperatures since many components will be dissipating power. Even the circuits within the smaller packages will be dissipating some power, and if this heat cannot be effectively removed, yet higher junction temperatures will be encountered. This next section examines the impact of temperature on circuits assembled in these new, smaller packages.

Thermal Considerations For Small Packages





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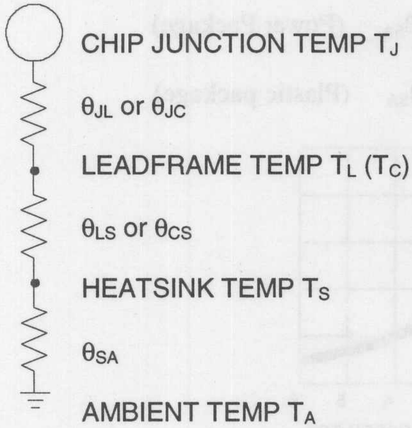
Modern manufacturing techniques and test methods for analogue I/Cs has reduced the possibility of receiving a device that fails to meet all specifications down to the level of a few part per million (ppm). Nevertheless some parts failure is still to be expected. As with other system hardware, the failure rate for I/Cs follows the familiar "bathtub" curve which plots failure rate versus time. The shaded area under the curve represents the failures associated with infant mortality caused by electrical overstress and/or excessive temperature. These failures are usually encountered during board assembly and testing and during the initial operation of the system. Careful engineering will minimise the failure rate from electrical overstress during the the second part of the curve and this is called the useful life. This period can extend from several years to decades until the onset of increasing failures from wearout. Both the failure rate during useful life and the onset of wearout are strongly affected by the operating temperature of the integrated circuit. Using high temperatures is a well validated method for accelerated life testing of integrated circuits. The acceleration factor with junction temperature is clearly shown in the second curve above, where the failure rate is normalised to 30 degrees Celcius . Note that a 10 degree increase from 100 to 110 degrees doubles the failure rate. Increasing the temperature to 120 degrees doubles it again.

Clearly, knowing and minimising the junction temperature of a circuit can prove to be important in ensuring the maximum reliability and lifetime of the part. Recognising this, integrated circuit manufacturers establish maximum permissable limits (Abs Max) for the junction temperature, similar to the electrical Abs Maxs used for current and voltage. They also include derating factors since the junction temperature not only depends on the operating ambient temperature, but also on the package and assembly method being used, and the internal heat (power dissipation) generated by operation of the integrated circuit.

Reliability is not the only issue. As many data sheets show, the operating specifications change with temperature, and a part that is within specification at normal room temperatures, may fall out of specification at higher temperatures encountered in the use of the part. For these reasons it is important that the circuit designer understands and evaluates the impact of temperature.

Integrated Circuit Thermal Nomenclature



$$R = V/I$$

then $\theta_{JA} = (T_J - T_A)/P_D$

θ = thermal resistance in °C/W
θ_{JL} = Junction to Leadframe
or θ_{JC} = Junction to Case (or Tab)
θ_{LS} = Leadframe to Heatsink
or θ_{CS} = Case to Heatsink
θ_{SA} = Heatsink to Ambient

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To help in using and interpreting the thermal data provided by National with its analogue integrated circuits, particularly with reference to the new, very small I/C packages that are being introduced, the following will review some thermal fundamentals, and then show how this information can be used in practical circuit designs.

First the buzzwords…

Thermal resistance is simply a useful figure of merit for heat transfer. For a system in thermal equilibrium (constant heat transfer from the semiconductor junction to the outside ambient air), an analogy is made to an electrical system where there is a constant flow of current in a resistor which is produced by the applied voltage. The heat flow is equivalent to the current flow, and the temperature differential is equivalent to the applied voltage. The most common symbol for thermal resistance is

$$\theta_{XY}$$

where the subscripts X and Y denote heat flow from X to Y. From our electrical analogy where

$$R = V/I$$

then

$$\theta_{JA} = (T_J - T_A)/P_D$$

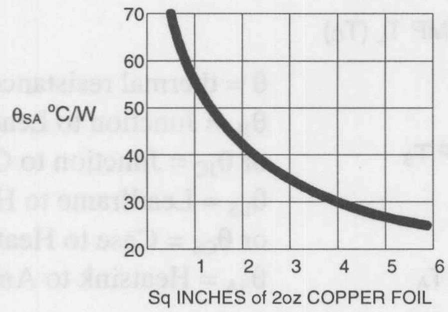
where T_J is the junction temperature, T_A is the ambient temperature, and P_D is the heat being dissipated. From this, the units for thermal resistance are clearly °C/W.

Free Air & System Thermal Resistance

With heatsinks:

$$\text{System } \theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \quad \text{(Power Package)}$$

$$= \theta_{JL} + \theta_{LS} + \theta_{SA} \quad \text{(Plastic package)}$$



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The total thermal resistance θ_{JA} is the sum of several components, all of which may, or may not, be significant or present. From the point of view of keeping the junction temperature as low as possible, small values for thermal resistance are desireable. For metal can, or plastic power packages with large metal tabs, the heat flows from the junction to the tab or case. Fairly effective heat transfer is possible and θ_{JC} can be as low as 1.5°C/Watt. For a plastic small signal package of the type we shall be dealing with here, the heat transfer is through the bonding wires to the lead frame, and is substantially less effective with thermal resistances θ_{JL} from around 45 °C/W and up. If a heatsink is available, there is a small thermal resistance θ_{LS} or θ_{CS} of the order of less than 0.25°C/W if soldered to the leads or tab, or up to 2°C/W if heatsink compound is used.

The thermal resistance of commercially available heatsinks for power packages can be less than 1°C/W , but for the surface mount packages used by small signal integrated circuits, the only practical method of heatsinking is to conduct the heat from the leads through the copper foil on the printed circuit board. The curve above shows the thermal resistances possible for single sided boards of 2oz copper.

Frequently, there is no practical possibility for additional heatsinking, and the system thermal resistance will be the same as the value quoted on the data sheet for the individual package. This value is measured without heatsinking and is known as the ***free air thermal resistance***. The package free air thermal resistance will be the most likely value used for the new small packages.

N.B

Sometimes the data sheet will quote other values for thermal resistance, e.g. when the part is soldered into a board with a stated area of copper foil. Curves may be found for several heatsinks of different thermal capabilities, including infinite heatsinks which imply the case or leads are held at the operating ambient temperature regardless of the level of internal power dissipation.

Small Package Thermal Resistance

PACKAGE	SIZE (MM)	θ_{JA} °C/W
microSMD	1.45 X 1.45	220
SC70-5	2 X 2.1	478
SOT23-5	2.9 X 3	265
MSOP-8	3 X 4.9	235
SOIC-8	4.9 X 6	165
TSSOP-14	5 X 6.4	155
SOT-223	6.5 X 7	174

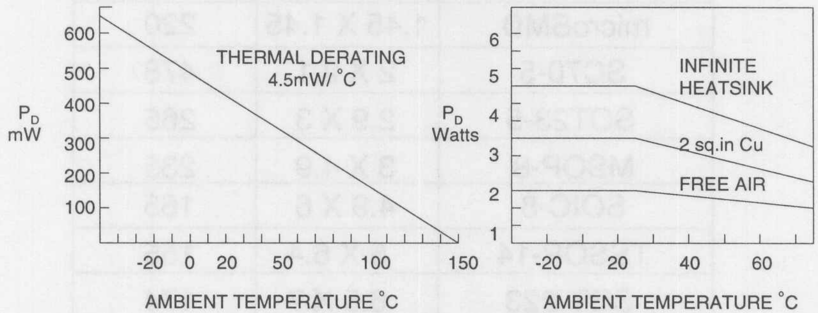
Notice that with these very small packages that the system thermal resistance (without heatsinking), will be the same as the package thermal resistance. Instead of tens of °C/W the thermal resistance is hundreds of °C/W. A note of caution, the numbers given above are typical only. There are several factors that impact the actual package thermal resistance. Obviously die size can change thermal resistance since a larger chip will have more area over which to dissipate the heat. Similarly the heat conductive properties of the bond wires and lead frame will give differences in packages assembled by different methods. Actual data sheet numbers may differ from the above quoted values for any given package by ± 15%.

It won't take much internal power dissipation (P_D) to drive the junction temperature (T_J) well above the operating ambient temperature (T_A).

Because the manufacturer has established a maximum limit for the junction temperature, the amount of internal power dissipation that is permissible must decrease as the operating ambient temperature (and hence the junction temperature) goes up. In fact by the time the ambient temperature is high enough that the junction temperature reaches its maximum, internal power dissipation must be reduced to zero. This fact allows us to introduce the concept of thermal derating and thermal derating factors.

Thermal Derating

$$\text{THERMAL DERATING} = \frac{1}{\text{THERMAL RESISTANCE}}$$

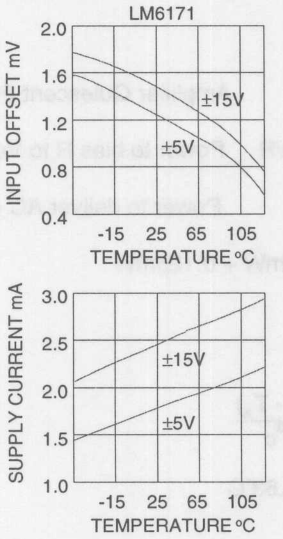


The units of the thermal derating factor are usually mW/ °C, and as such the derating factor bears a direct relationship to the more commonly quoted thermal resistance. The factor indicates the amount by which the internal power dissipation of the IC must be reduced for each degree increase in junction temperature such that, by the time the maximum junction temperature is reached, the internal power dissipation is reduced to zero.

A popular way to use the derating factor is to construct a graph of P_D versus ambient temperature as shown in the Figure on the left. For any given level of P_D, it is a simple matter to read off the maximum allowable operating temperature. For the example shown here, if the device dissipation is 200mW, then the part can be operated in a 90°C ambient without exceeding the maximum junction temperature of 150°C. Any operating point for power dissipation and ambient temperature under the curve will meet this criterion. Nevertheless, as we shall see later, this may not be the most important criterion.

The second set of curves shows alternative ways of presenting the data. When it is possible to heatsink, additional lines can be drawn. These are often labeled with the size of the heatsink being used, but if necessary, the derating factor can be calculated from the slope of the line. Although the curves can be extrapolated to temperatures below 25°C, conventionally the power dissipation is held constant at the 25°C level. Also the ambient temperature range is not continued out to the maximum junction temperature (the temperature at which all the lines meet), but instead terminates at the maximum anticipated operating ambient temperature. That temperature depends on whether the part is designated for Commercial, Industrial or Military use with a range from 70°C to 125°C for most Operational Amplifiers. The steepest slope is for the infinite heatsink and simply represent the thermal resistance, junction to case, for the package.

Temperature & Specifications



OPERATING TEMPERATURE

FULL RANGE

$$-40^{\circ}C < T_A < +85^{\circ}C$$

$$T_A = T_J$$

$$-40^{\circ}C < T_J < +85^{\circ}C$$

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It might seem from the foregoing that exceeding the maximum junction temperature is the biggest problem that confronts the designer when using parts at elevated ambient temperatures, and the relatively high thermal resistances of small packages combined with the inability to provide effective heatsinking further exacerbates the problem. In point of fact, this is not the case as a few practical examples will show.

Temperature not only affects reliability, it also has an effect on the performance specifications. Most data sheets include typical curves with temperature as one of the co-ordinates, to show how the specification changes with temperature. To further assist designers in assessing the effects of temperature, data sheets provide specification limits for various parameters at elevated ambient temperatures. For National, **boldfaced** limits apply for the specified temperature range.

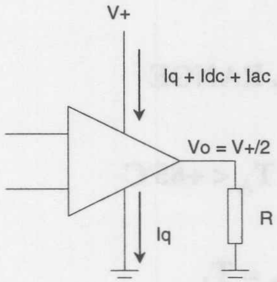
These temperature ranges are the ones usually associated with Industrial or Military use. On data sheets from many manufacturers this appears as

$$-40°C < T_A < +85°C \quad \text{and} \quad -55°C < T_A < =125°C$$

and sometimes the words operating temperature or full range are used instead of T_A. In other cases a footnote is added stating $T_A = T_J$. Without this footnote, the actual temperature limits in each of the above cases can be misleading, since it implies that the specification limit will not be exceeded while operating at these temperature extremes. Most National data sheets list the temperature range by T_J. This is because when the parameter is tested at elevated temperatures, the test time is too short to allow internal power dissipation to raise the junction temperature above that ambient. In effect, the part is being tested at a junction temperature the same as that ambient temperature. In actual operation, internal power dissipation may mean the junction temperature is higher. If it is significantly higher, strictly speaking the spec limit may not apply.

In practical terms, high volume/high speed testing, and no pre-knowledge of the actual power dissipation, prevents measurements at sustained high temperature operation, further emphasising the need to provide adequate guard bands for performance specifications.

Calculating T_J



$$P_D = V^+ \times Iq \quad \text{Amplifier Quiescent Power}$$

$$+ (V^+ - Vo) \times Vo/R \quad \text{Power to bias R to Vo}$$

$$+ (V^+)^2/20R \quad \text{Power to deliver AC swing}$$

$$= 1.75\text{mW} + 0.625\text{mW} + 0.125\text{mW}$$

$$= \underline{2.5\text{mW}}$$

T_A (max) = 85°C
V^+ = 5V
Iq (max) = 350uA
θ_{JA} (SOT23-5) = 265°C/W

$$\theta_{JA} = \frac{(T_J - T_A)}{P_D}$$

$$= 85.63°\text{C}$$

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Analog Solutions 26

Before anyone panics and concludes small packages are going to be hard to use (let alone too hard to see), we'll go through a couple of examples to see exactly what we are dealing with.

Example 1

An LMV321 Operational Amplifier in a SOT23-5 package is being used to buffer a 1kHz sine wave into a 10 kilohm load with an output biassed to half the supply voltage, which is 5V. It is expected that the equipment will have to work in a maximum ambient temperature of 85°C. Calculate the worst case junction temperature for the amplifier.

Solution

From the data sheet for the amplifier, at a junction temperature of 85°C, and a 5V supply, the maximum supply current Iq is 350uA. The thermal resistance for the SOT23-5 package with this amplifier is given as 265°C/W.

1) Calculate the value of P_D:

P_D = Amp Quiescent Power + Power to bias load to $V^+/2$ + Power to swing signal in the Load

$$PD = 5 \times 350\text{x}10^{-6} + (5-2.5) \times 2.5/10^4 + 5^2/20 \times 10^4$$

$$= 1.75\text{mW} + 0.625\text{mW} + 0.125\text{mW}$$

$$= \underline{2.5\text{mW}}$$

2) Calculate TJ:

$$\theta_{JA} = (T_J - T_A)/P_D$$

$$265 = (T_J - 85)\ 2.5\text{x}10^{-3}$$

Therefore $T_J = \underline{85.63°\text{C}}$

Contributions to Power Dissipation

♠**SUPPLY VOLTAGE** ***Is it above 10 Volts?***

♠**QUIESCENT CURRENT** ***Is it above 1mA?***

♠**LOAD** ***Is it less than 600 ohms?***

♠**LOAD** ***Is it ac or dc coupled?***

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Analog Solutions 27

Because of low supply voltages and relatively large load resistors used in many applications, the effect on T_J for most designs will be similar to this a very slight increase over the ambient, and certainly too small to be of concern. Will this always be the case? Here are some pointers on what to look out for.

1) Supply Voltage	Is it above 10V-15V?
2) Load	Resistive or reactive and less than 600 ohms?
3) Load	AC or DC coupled?
4) Quiescent current	Above 5mA?

Although the impact was negligible in the previous example, look at how much power dissipation was caused simply to bias the amplifier……70% of the total

to bias the output………25% and to drive the load………..5%

Example 2

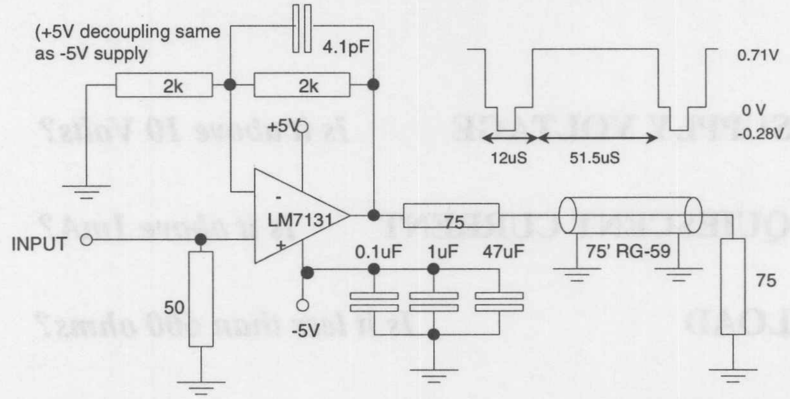
An LM7131 is being used as a cable driver for a dc coupled video signal which has a voltage swing from -0.28 volts (at sync tip) to +0.71 volts (at peak white). The cable is back matched with its characteristic impedance of 75 ohms. Assuming a maximum operating ambient temperature of 70°C and a peak white video signal, what is the maximum junction temperature of the LM7131 in the SOT23-5 package?

Solution 2

To accommodate the below ground voltage swing of the signal, split power supplies are needed, and the LM7131 is characterised with 5V supplies (ie V+ = 5V, V- = -5V). From that section of the data sheet, the quiescent current at a 70°C temperature is 10 mA maximum.

The average dc value of a peak white video signal with a 12us blanking period and a 52us active video period is 0.57 volts. Since the cable is back matched, the LM7131 will need a gain of two and will be driving a 150 load with an average level of 2 x 0.57 = 1.14 volts.

Video Cable Driver



T_A (max) = 70ºC
Iq (max) = 10mA
Av = 2
R = 150 ohms
Supply = 10Volts

P_D = 100mW + 29.3mW = <u>129.3mW</u>

θ_{JA} = 325ºC/W

T_J = 112ºC

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Analog Solutions 28

1) Calculate the value of P_D.

$$P_D = (V^+ + V^-)\, Iq \ + \ (V^+ - V_S) \times V_S/R$$

$V^+ = V^- = 5V$

V_s = Average dc value of signal at output

= 1.14 Volts

R = 75 + 75 = 150 ohms

Therefore PD= 100mW + 29.3mW = <u>129.3 mW</u>

2) Calculate T_J.

$$\theta_{JA} = (T_J - T_A)/P_D$$

$$325 = (T_J - 70)/129.3\times10^{-3}$$

$$T_J = \underline{112°C}$$

Now the assumption that $T_J = T_A$ is not justified and is, in fact, some 27°C higher than the measurement temperature used in the data sheet. Under these circumstances the maximum limits guaranteed by the data sheet may not be met. Even so, the junction temperature is still well below the Abs Max of 150°C, so device reliability will not be changed very much.

Reducing T_J

DEVICE	PACKAGE	T_J (max)
LM 7131	SOT23-5	112°C
	SOIC-8	91.3°C
	DIP	85°C
LM 6171	SOIC-8	81°C

Again, the dominant source of heat is from the amplifier quiescent current and the supply voltage. In this case, although the load is dc coupled, because split power supplies are used no power dissipation is incurred in order to bias the output stage. While the power dissipation from driving the load has gone up, it is still less than 25% of the total.

For a very conservative design, there are several alternatives available to reduce the junction temperature. The simplest is to use a package with a lower thermal resistance. The 8 pin SO8 will drop the junction temperature to 91.3°C, a mere 5.3°C above the guaranteed spec limit. A through hole DIP will bring the junction temperature down to 85°C, but may not be compatible with a board design using surface mount devices.

Noting that the device itself provided the largest contribution to heat dissipation, other types may offer better performance in this respect. For example, the LM6171 offers the same speed but with a maximum supply current at elevated temperatures of only 3.5mA. In the SO8 package, the worst case junction temperature is 81°C, well under the guaranteed limit.

LOW VOLTAGE/LOW POWER OP AMPS...

HELPING MAKE THE INFORMATION AGE PORTABLE

System Voltage Levels Driven Lower By;

- **Digital system requirements for greater speed for processing information**
  - greater speed requires finer processing geometry
  - finer geometry means lower breakdown voltage
  - lower 1 to 0 voltage transitions result in faster data rates
- **Portability of computing and communications**
  - single cell becoming stack configuration of choice
- **Analog I.C.s respond to voltage levels driven by digital requirements**

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Analog Solutions 31

The development of lower and lower rail voltages is a fact of equipment design that applies to a very broad range of applications and market segments. But what are the factors that drive this migration to lower and lower voltages?

Basically, two factors converge to drive rail voltages from +5V, to 3.3V, to 3.0V, to 2.7V etc. These are the need for speed in digital circuits for the purpose of processing information, and the availability of batteries with terminal voltages at either 1.5V or 4.1V. Stack combinations define the available supply voltages for portable equipment. Single cell-designs are increasingly popular. Single-cell end of life voltage puts the low end +rail voltage at about 1.8V.

Digital I.C.s can process signals faster if the geometry of the transistors is small. Small geometry transistors in an I.C., leads to lower breakdown voltage. So speed drives lower supply voltage. The theoretical limit of voltage for the purpose of the information that is being carried has not been approached, if in fact it exists at all. The limits that represent the current state of the art are determined by process lithography, and the capability of clean room equipment and techniques, and transistor saturation characteristics. Also, a lower 1 to 0 or 0 to 1 excursion in terms of voltage allows ultimately for faster data processing. Consequently digital I.C. processes intended for high speed set the system voltages to be used.

Analog I.C.s, such as op-amps, comparators and converters are responding with low voltage designs that serve these new realities.

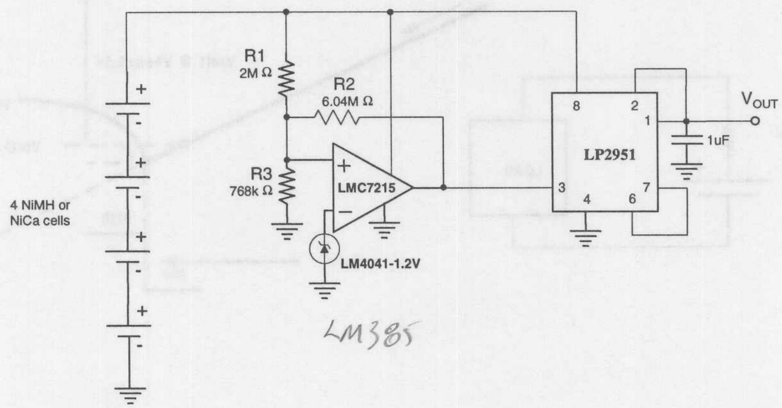
Low Voltage/low Power Applications

- Min. Battery Voltage Detector with Load Disconnect
- Micropower V-to-F Converter
- New Low-voltage bipolar op-amp series
- LMV822 Telephone Line Transceiver Application
- Low voltage squaring circuit

National Semiconductor

Many of National's newest amplifiers IC's are designed for use in battery and low voltage systems. Following is a collection of applications circuits that employ new devices from National Semiconductor's Analog group.

Min. Battery Voltage Detector With Load Disconnect(LMC7215)



LM385

National Semiconductor

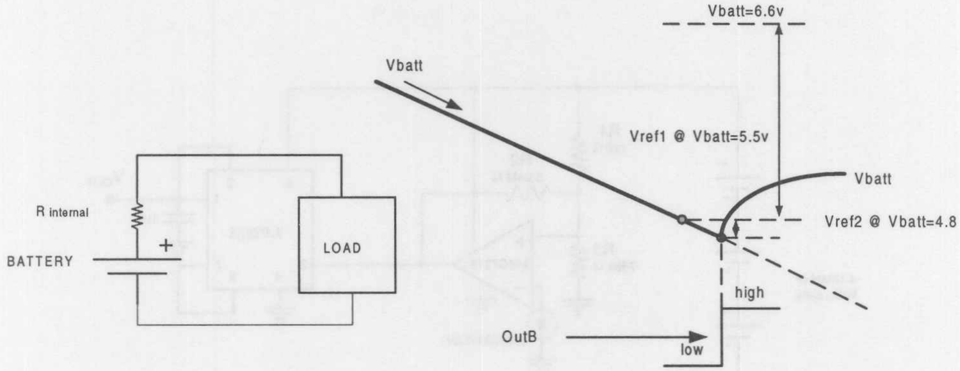
Analog Solutions 33

Many portable systems use rechargeable batteries. A key circuit application for rechargeable batteries is voltage level detection.

The above circuit protects the batteries from harmful over-discharge by monitoring the battery voltage. When the battery drops to a minimum level, it disconnects the load by pulling the ON/OFF input of the LP2951 low. R1, R2 and R3 work together to set the trigger level and to provide hysteresis. Trigger level occurs when the battery voltage drops to a level equal to the reference voltage. The hysteresis range is set for 1.2 V to account for the battery recovery voltage.

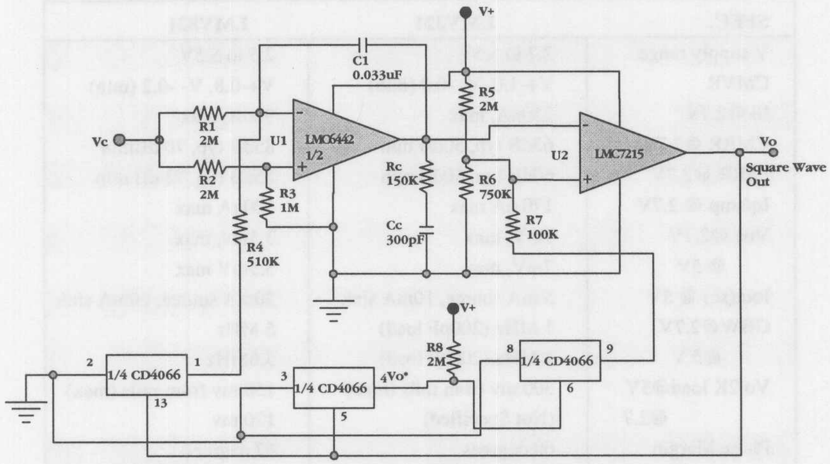
The LMC7215 is well suited for such an application because of its micro-power(1uA/comparator), its ultra-low input current (1fA), its rail-to-rail output, and its supply voltage range (1.8 V to 8 V)

Load Disconnect Considerations



The previous circuit used a relatively large hysteresis voltage (1.2 V) to compensate for the internal resistance of the battery. When the battery is connected to the load, its voltage equals its unloaded voltage minus the IR drop across the internal resistance. When the load is disconnected, the battery voltage jumps back up because there is no load current to create a voltage drop across the internal resistance.

Micropower V To F Converter



Using the LMC6442 CMOS op-amp and its micropower voltage comparator counter-part, LMC7215, with 0.7uA of supply current, it is possible to build subsystems which consume a fraction of the power consumed in earlier designs.

The circuit shown above is a voltage to frequency converter built with said components and a quad analog switch, CD4066. The total supply current with a single 5V supply is less than 10uA nominal. The input voltage (Vc) range is 0 to 10V with the components shown and the output linearity is better than 1% over that range. With the components shown, the input-output transfer characteristics is set to about 4.3Hz/V. There is an upper frequency limit of operation of about 50Hz due to the bandwidth limit of the LMC6442 before the transfer function non-linearity becomes excessive.

U1 is a triangle wave generator which alternatively swings between the two distinct threshold levels set by U2. Rc and Cc were added to insure stability since with a capacitor in the feedback loop, U1 is effectively operating in a unity gain configuration (see the LMC6442 data sheet for stability considerations and compensation techniques). The output has almost full rail-to-rail swing capability.

National's LMV series Op-Amps
800 Series vs 300 Series

SPEC.	LMV321	LMV821
V supply range	2.7 to 5.5V	2.5 to 5.5V
CMVR	V+-1.0, V- -0.0 (min)	V+-0.8, V- -0.2 (min)
Ib @2.7V	250nA, max	90nA, max
CMRR @2.7V	63dB typ, 50dB min	85dB typ, 70 dBmin
PSRR @2.7V	60dB typ, 50dB min	85dB typ, 73 dB min
Iq/amp @ 2.7V	170 uA max	300uA max
Vos @2.7V	7mV, max	3.5mv, max
@ 5V	7mV, max	3.5mV max
Iout(sc) @ 5V	5 mA source, 10mA sink	20mA source, 20mA sink
GBW@2.7V	1 MHz (200pF load)	5 MHz
@5V	1MHz (200pF load)	5.6MHz
Vo 2K load@5V	300 mv from rails (max)	150 mv from rails (max)
@2.7	(Not Specified)	120 mv
Phase Margin	60 degrees	67 degrees
Package	SC-70, SOT 23-5	SC-70, SOT 23-5
Slew Rate	1 V/us typ	1.4 V/us min

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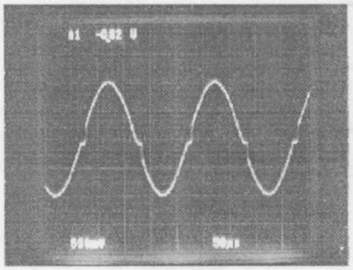
Analog Solutions 36

LMV321/358/324 and LMV821/822/824

No Crossover Distortion

Output Swing of **LM324**

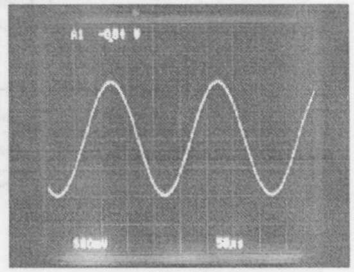
500mV/div



50µs/div

Output Swing of **LMV324**

500mV/div



50µs/div

V_S=+/-2.5V, A_V = +1

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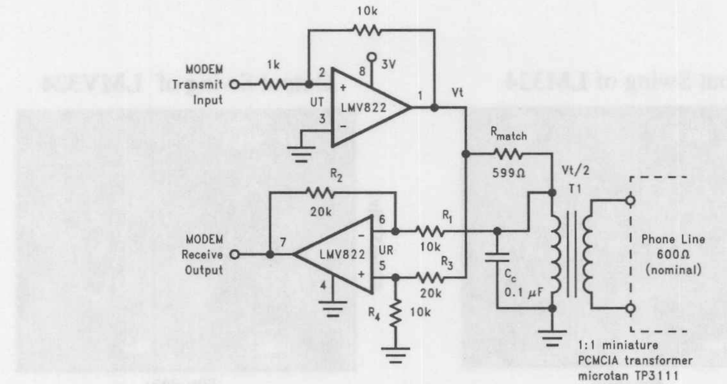
The scope photos above compare the output swing of the conventional LM324(left) and the new improved LMV324(right) powered with a 5V supply.

The existing LM358/324 has a class B push-pull complementary output stage with current limiting. They have been designed mainly for sourcing current. When the op-amp is asked to sink and source current, crossover distortion is introduced at the output because of the two base emitter voltage drop (3Vbe) between the NPN (sourcing current) and the PNP (sinking current) transistors. See the scope photo above, left. When lower power supply voltages are used, the signal swings are smaller and any crossover distortion will become a larger component of the overall distortion level. With an improved output stage, the new LMV321/358/324 eliminates the output crossover distortion effectively. See scope photo above, right.

LMC822 Telecomm. Application
A Telephone Line Transceiver



$$V_O = V_T\left(\frac{R_3}{R_3+R_4}\right)\left(1+\frac{R_2}{R_1}\right) - \frac{V_T}{2}\left(\frac{R_2}{R_1}\right) = V_T\frac{1}{3}(3) - \frac{V_T}{2}(2) = 0$$

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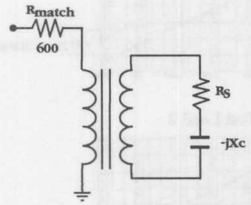
Analog Solutions 38

The above circuit is one of many possible topologies that the telecommunications community uses to interface phone line equipment (MODEM, telephone, etc.). It is basically an audio (300Hz to 3kHz) transceiver with echo cancellation. The receiver portion UR can receive while UT Transmits; ie, it is full-duplexed. UR is configured to cancel out UT's output by taking the difference between V_T and $V_T/2$ (Rmatch divides V_T by two). The differencing is weighted via R1,R2, R3, and R4 to cancel this input difference signal: (V_T-$V_T/2$).

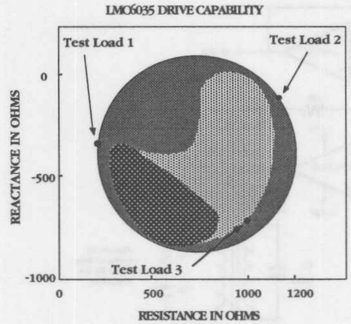
Because of its many possible configurations, the telecomunity refers to it as "the hybrid". The above version of the hybrid uses National's dual op-amp LMC6035's unique fit in meeting the transmit requirements, in low voltage telephone transceiver applications PCMCIA modem cards for example.

The ever increasing demand for low voltage systems (telephone systems in particular) places new demands on established applications. The LMV822 was produced to meet such a demand.. It is able to provide good low voltage performance over a broad range of parameters. But one parameter makes the LMV822 particularly desirable for the above application is its output swing capability into heavy loads. Like all telephone "hybrid" circuits, the above version is required to drive the nominal phone line load of 600Ω. The LMC6035 drives 600Ω load 0.2V from the rails (guaranteed).

Phone Line Simulations



Test Load#	Coordinates @1kHz	R_S	C_S
1	220Ω-j288	220Ω	552nF
2	1.2kΩ-j108	1.2kΩ	1.48uF
3	1.0kΩ-j758	1.0kΩ	3210nF



Range of high occurence of phone line input impedance

Range of medium occurence of phone line input impedance

Range of low occurence of phone line input impedance

The LMV822 was measured for its phase margin performance when applied to the previous phone line transceiver application. Focusing on the transmitter portion (UT), AC gain/phase measurements were taken while the LMV822 drove Rmatch, T1 and three different possible phone line loads. These simulated (dummy) loads were obtained from the circular chart shown in the above slide. It is an impedance circle, and it covers the the various impedance possibility for different phone lines. The y-axis covers a range of reactive loading while x-axis covers a corresponding range of resistive loading.

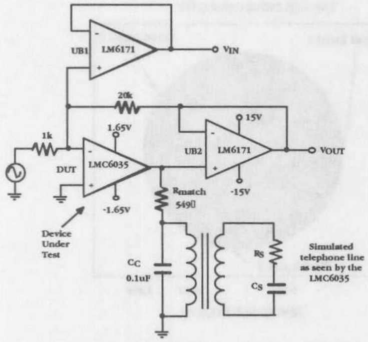
The impedance circle is used for choosing three different possible phone line loads. These three selections were chosen along the perimeter of the circle with the intent of encompassing a vast range of possibilities. The chosen impedance points are indicated by number above. The associated series RC values are also shown.

Once these values were determined, they were used to measure the LMC6035's phase margin performance proving out its performance in telephone hybrid applications. Note that the transformer was a miniature, PCMCIA type, a common low voltage platform.

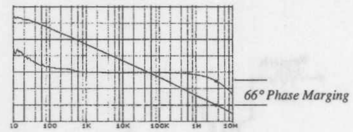
The test circuit for measuring loaded gain and phase over frequency is shown on the following slide. Also shown, are three Gain/Phase plots (measurements). Each curve is numbered according to the numbered impedance points on the above impedance circle.

For more details see App. Note AN397.

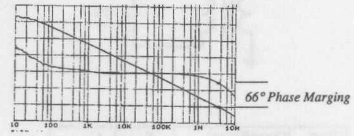
Phase Margin Measurements Over a Vast Range
Phone line loads



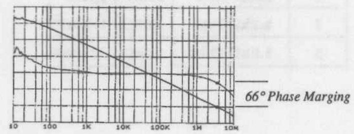
Test Load 1



Test Load 2



Test Load 3



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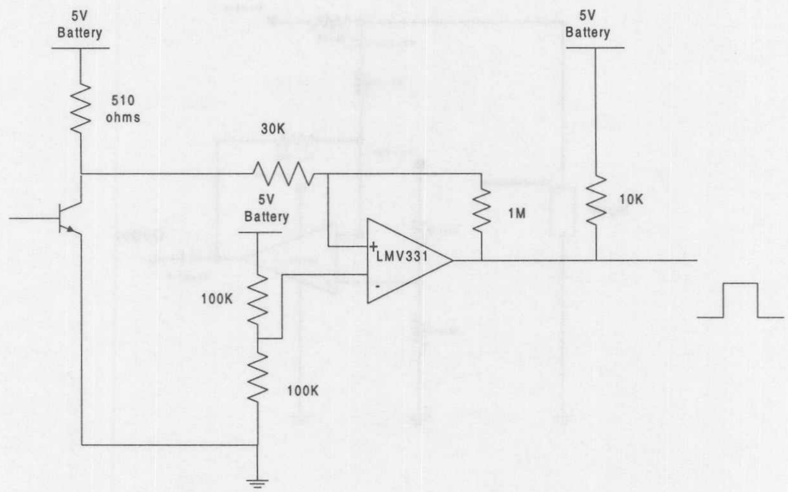
Analog Solutions 40

The above shows the test circuit. The three, previously described RC combinations are represented by how they effect the LMV822 's phase margin over a vast range of phone line possibilities. The phase margin is indicated for each graph. The graphs are numbered according to the numbered test loads shown in the previous slide.

Squaring Circuit



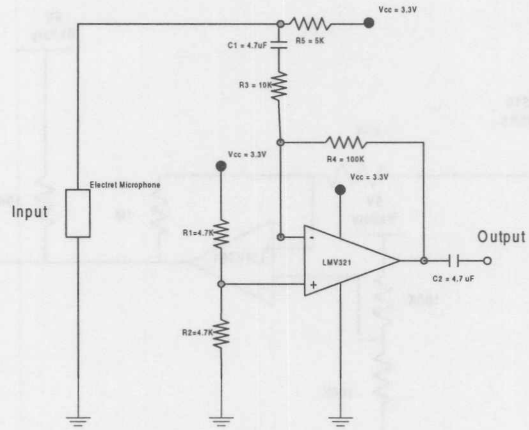
This a quick, easy, and cost effective solution for generating a square wave from a sinusoidal signal.

This application can run from a battery voltage of 2.7V to 5V. The input is a sinusoidal or other signal that is amplified by the discrete transistor and sampled by the low power LMV331 device.

The output is pulled up with a 10K resistor to generate rail to rail output. The square wave output can be fed into a microprocessor.

This circuit has 150 mV of hysteresis to prevent the comparator from oscillating. A basic comparator configuration may oscillate or produce a noisy output if the applied differential input is near the comparator's offset voltage. This usually happens when the input signal is moving very slowly across the compartor's switching threshold.

Microphone Preamplifier



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Analog Solutions 42

Many of our latest packages are smaller than the discrete components that surround them. Since resistors are easily integrated (and small capacitors under 50pF) the circuit shown here can be reduced to a circuit board size not much larger than that of a single surface mount resistor.

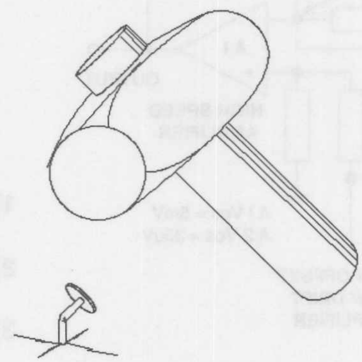
Here is an electret microphone preamplifier. Since the output of an electret microphone is a low level output, a preamplifier is used to amplify the signal.

Electret microphones require an external D.C. voltage source to bias the microphone. Typically, the biasing is performed through the output of the microphone. A capacitor C1 is placed between microphone output and the inverting input of the Op Amp to block the D.C. offset to the Op Amp.

The Op Amp uses resistors, R3 and R4, to configure the Op Amp as an inverting amplifier with a closed loop gain of 100 (20dB). A voltage divider between resistors, R1 and R2, sets the reference half way between the Vcc and ground.

THE SEARCH FOR PRECISION

THE LMC2001



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Analog Solutions 43

What makes a precision Op-Amp? Primarily high dc open loop gain combined with low input offset voltages and offset bias currents. In particular the offsets should not drift with temperature changes, or over a period of time. Although the conventional Op-Amp has improved characteristics over many years of development, to the point that many precision applications can be satisfied quite easily, some of the more demanding applications have required a stabilised Op-Amp, where special circuit techniques are used to minimise offsets and eliminate the drift in characteristics that occur at initial turn-on and over a long period of continuous operation.

In the search for precision, many approaches to stabilisation have been taken, but since nearly all stabilised amplifiers are actually composite amplifiers, ie a combination of two amplifiers with different characteristics, in describing how the LMC2001 works, this is where we will start.

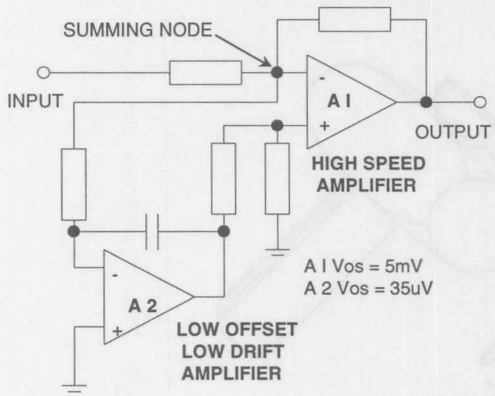
The Composite Amplifier

Although the "ideal " Op-Amp has been described many times, quite often that description has been arrived at by taking some parameters, such as bandwidth, input impedance, gain etc, and increasing them to infinity, while taking other parameters, such as output impedance, offset, price etc, and reducing them to zero. More practically, Op-Amps have evolved with steady improvements in either a single parameter or in several, sometimes at the expense of others, to better suit the amplifier for a given range of applications.

In the case of the precision Op-Amp, wide bandwidth is frequently sacrificed to obtain good performance at or close to dc. Nevertheless, some precision applications require high closed loop gain along with a reasonable closed loop bandwidth. A 1MHz GBW may seem to be pretty impressive, but with a closed loop (signal gain) of 40dB, the closed loop bandwidth is only 10kHz, and for low distortion, the signal bandwidth is much less, closer to 1kHz!

High GBW amplifiers are available (5 MHz), but, for unity gain stability, these usually have lower dc open loop gain (110dB) than would be suitable for precision applications, and have offsets that are an order of magnitude too high (1-5mV).

Composite Amplifiers



1) Inverting only

2) Vos ≠ 0

3) Drift = Drift of A 2

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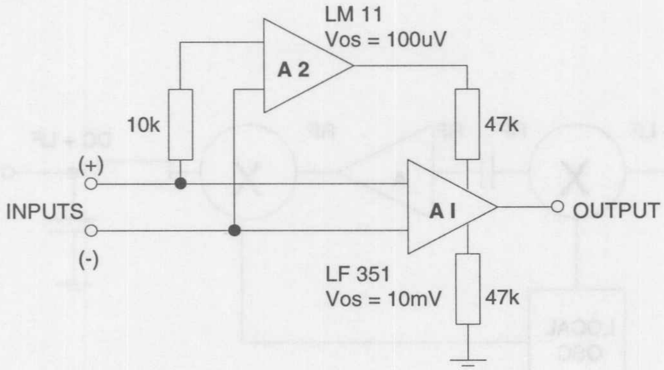
Analog Solutions 44

The composite amplifier shown above, resolves this dilemma by connecting two amplifiers in parallel across the signal input. A1 is a high speed amplifier with modest dc characteristics. A2 is a low speed amplifier with low input offsets and low drift.

For A1 alone, with the non inverting input connected to ground, for zero signal input the output should be at ground potential, and hence the inverting input will be at ground. This is the ideal case when there are no offsets. However, if A1 has an input offset voltage of 5mV, the output will have to move to put the inverting input 5mV away from the non-inverting input. With a closed loop gain of 40dB, the output then has to move 500mV away from ground instead of remaining at zero. In the composite amplifier, A2 inverting input is also connected to the summing node, with its non inverting input connected to ground. However the offset voltage for A2 is only 35uV, and if the output of the composite amplifier moves the summing node more than 35uV away from ground potential, this difference, multiplied by the dc open loop gain of A2, will appear at the output of A2 and be applied the non-inverting input of A1. In essence then, the output of the composite amp will only move far enough to put the summing junction 35uV away from ground. With a closed loop gain of 40dB, this is only 3.5mv compared to the 500mV for A1 alone.

There are a several clear -and not so clear- disadvantages to this stabilisation technique. Since the non-inverting input of A1 is used to provide the correction signal, the composite amplifier can be used only in the inverting mode. The offset is still not reduced to zero, and can still drift with time and temperature (dependent on the offset and drift characteristics of A1).

Improved Composite Amplifier

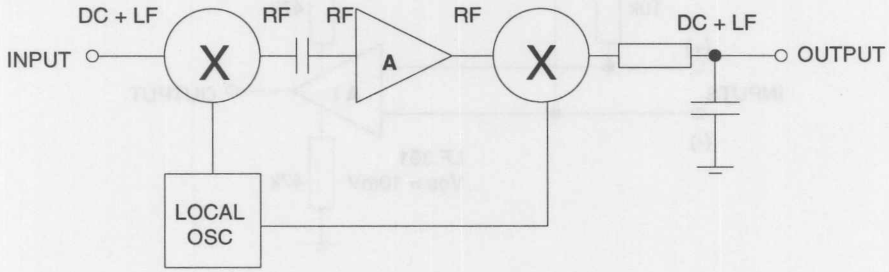


Dealing with the first disadvantage, if the high speed amplifier A1 has input offset adjust pins, then these can be used as the point to apply stabilisation, and the composite amplifier can be used in either inverting or non-inverting modes.

This is shown above, where the composite amplifier is comprised of an LM11 (input offset current 0.5pA, input offset voltage 100uV, long term stability 10uV/year), and an LF351 (GBW 4MHz, input offset 10mV). Application of a feedback network from the output to the inverting input will set the composite amplifier closed loop gain in the conventional way.

Using offset pins on the high speed amplifier easily resolves one problem (actually the LMC2001 does this slightly different way, as we shall see later), but the big problem, that of the offset and drift of the low speed amplifier, while greatly reduced compared to the performance of the high speed amplifier, still remains.

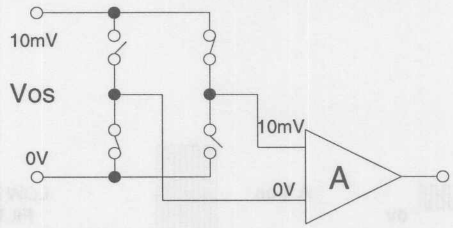
DC and L.F Modulation



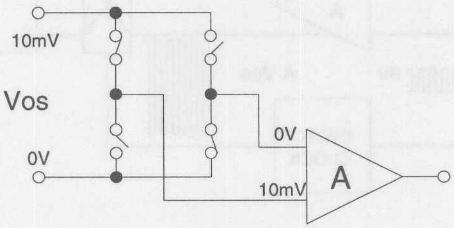
In a seeming paradox, the solution is to use an ac amplifier for the low speed path. Since the signal is ac coupled through the amplifier, any dc offset voltages present in the ac amplifier are completely ignored, as will any drift of these dc terms. But since we are trying to correct the dc and low frequency (drift) offset of the high speed amplifier, how is the ac amplifier able to measure this dc and l.f and use it to generate a dc correction?

The answer is to convert the dc and low frequency terms to a high carrier frequency such that the amplitude of the carrier frequency is the desired information (the modulation). Upon demodulation, the carrier amplitude or signal dc content is recovered without any added dc or low frequency contributions from the processing amplifier.

LMC2001 Input Switch Bank



a) First switch position

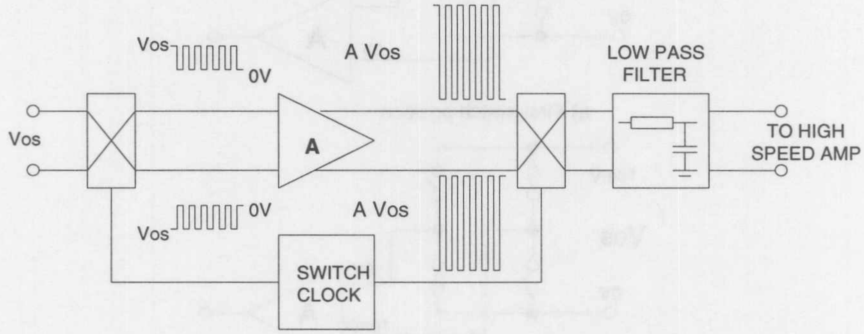


b) Second switch position

The dc offset (Vos) and low frequency components (offset drift and 1/f noise) from the high speed amplifier are coupled to a switch bank, above, which applies the signal to first one side of the ac amplifier, and then to the other side at a rate set by the clock frequency.

The resulting input to the amplifier is, therefore, an ac waveform with a period set by the clock, and an amplitude that is determined by the dc level at the input to the switch bank.

LMC2001 Low Speed (Precision) Amplifier



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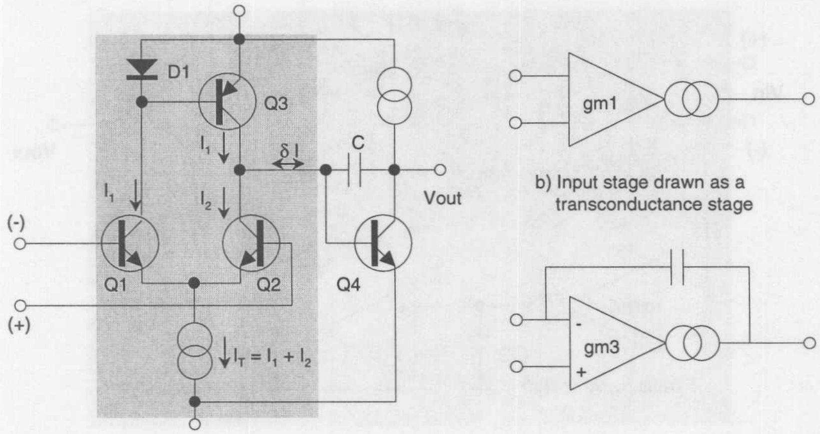
As the input offset voltage increases, so will the amplitude of this ac waveform increase. After the waveform has been amplified, it is demodulated to recover the amplitude of the modulation, which is the now the amplified dc offset of the high speed amplifier. Any dc or low frequency components caused by dc offsets or drift in the precision amplifier are ignored by the demodulation process since they did not add to the ac amplitude. The detected voltage is then passed through a low pass filter to remove any remaining high frequency components such as the carrier frequency and switching harmonics, and is applied to the high frequency amplifier to cancel the composite amplifier dc and low frequency offsets.

Clearly, the input to the precision low speed amplifier is from the input terminals of the high speed amplifier. Before showing how the output of the precision amplifier is used to correct this offset voltage, we need to look at transconductance, or gm stages.

Transconductance Amplifiers



a) Basic Op-Amp

c) Output stage

There is no mystery to transconductance stages. In fact, as shown here, the the basic Op-Amp consists of an input transconductance stage. The input voltage is converted to an output current by the action of the transistor differential pair and the current mirror load. Under balanced conditions, the transistor currents I1 and I2 are equal. Since Q1 current is mirrored to the collector of Q2 the net current to the output stage is zero. When a differential signal exists (either a desired signal or an offset voltage) there will be a difference current dI, which will be passed to the output stage. The input stage transconductance gm1 is therefore given by

$$gm1 = \delta I/Vin$$

For convenience we can redraw the input stage as shown in b). The Op-Amp output voltage is the result of this difference current flowing in the compensation capacitor C, ie

$$Vout = \delta I/jwC$$

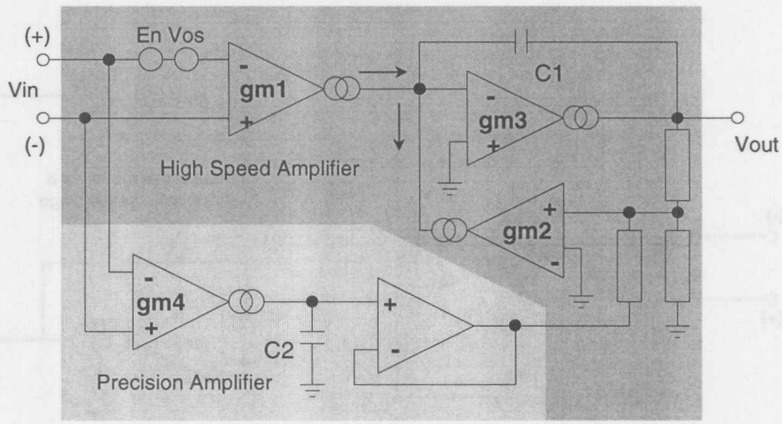
giving the very simple expression for the ac open loop gain as

$$Vout/Vin = gm1/jwC$$

This single dominant pole response is smooth and can be well controlled in the IC process, which, as we will see, is important in providing a smooth response for the LMC2001 composite amplifier.

The amplifier output stage can also be redrawn as shown in c), as a transconductance stage with an integrating capacitor. Not shown is the unity gain voltage buffer to provide a low output impedance.

LMC2001 Block Diagram



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We now have all the elements to show the full block diagram of the LMC2001. Transconductance stages gm1 and gm3 comprise the high speed amplifier, and the modulator/demodulator are combined in the transconductance block gm4 to represent the low speed precision amplifier. Another transconductance stage, gm3, helps provide the dc open loop gain of the high speed amplifier, and also performs as a summing junction for the offset correction voltage.

When the external feedback loop is closed, in the absence of an offset correction, any imbalance in the high speed amplifier input stage (unequal sharing of the tail current from Vbe mis-match, imperfect matching in the current turn around etc) will generate an offset current output when the input voltages are equal. With external feedback this will cause the high speed amplifier output to move away from zero in order to provide the necessary input voltage differential to restore balance. With the low speed amplifier connected to the same inputs, this voltage will also be applied to the input of the low frequency stage and multiplied by the dc gain of this stage, converted to a current, and summed with the offset current from the high speed input stage, canceling this current.

To see how much this reduces the composite amplifier offset, consider that, without stabilisation, the first stage output current is

$$\delta I = gm1 \times Vos1$$

where Vos1 is the offset voltage of the high speed amplifier stage.When stabilisation is applied the output current from the low speed stage is

$$\delta I' = Vos2 \times gm4 \times R \times gm2$$

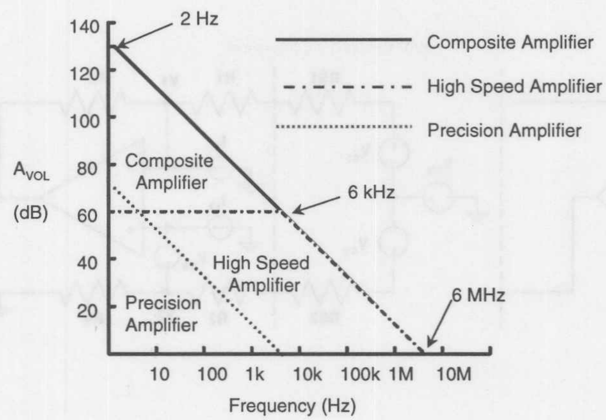
where Vos2 is the offset after stabilisation. Since after stabilisation,

$$\delta I' = \delta I$$

$$\text{then } Vos2 = Vos1 \times gm1 / (gm2 \times gm4 \times R)$$

In the case of the LMC2001, this gain ratio reduces the offset due to the high speed input stage by nearly 110dB!

Open Loop Response of the LMC2001

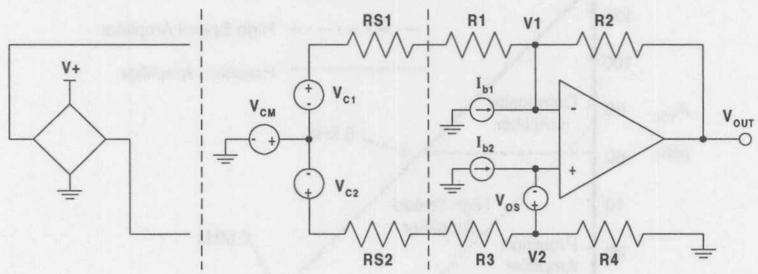


A not so obvious problem with composite amplifiers is matching the frequency/gain responses of the two amplifiers to produce a smooth overall response. In the LMC2001 both amplifiers are fabricated on the same die, producing excellent matching as shown here.

Each amplifier has a single dominant pole so the ac gain for both falls at a -6dB/octave rate. The corner frequency for the high speed amplifier is set at 6kHz (dashed line), whereas for the low speed amplifier this pole frequency is at 2Hz (dotted line). The gms' of the two amplifiers are also matched to produce a pole/zero cancellation, ie the open loop gain of the low frequency amp falls to 0dB at the same frequency as the high frequency amplifier pole frequency (6kHz). This produces the smooth overall response of the composite amplifier shown as a solid line. The ac gain falls at a -6dB/octave rate through the entire useable frequency range. The combined open loop gain is 130dB, well within the range for precision applications and the 6MHz unity gain crossover frequency allows wide signal bandwidths at high closed loop gain.

Such a combination of speed and precision makes the LMC2001 a versatile operational amplifier. Now we will look at some circuit applications that can take advantage of such performance.

The Difference Amp



In the real world analog signals come packaged with an assortment of undesired signals. Typical of these are signals from transducers and we will look at some transducers and different ways to extract the desired signal.

Pressure transducers, load cells, strain gages, etc. are usually in a four resistor bridge that generates a signal called a common mode signal, and the desired signal, called a normal mode signal. Any text book describing an operational amplifier, or op amp, starts with the inverting and non-inverting configurations, and proceeds to the four resistor difference amplifier. With the introduction of new op amps, this configuration is worth considering.

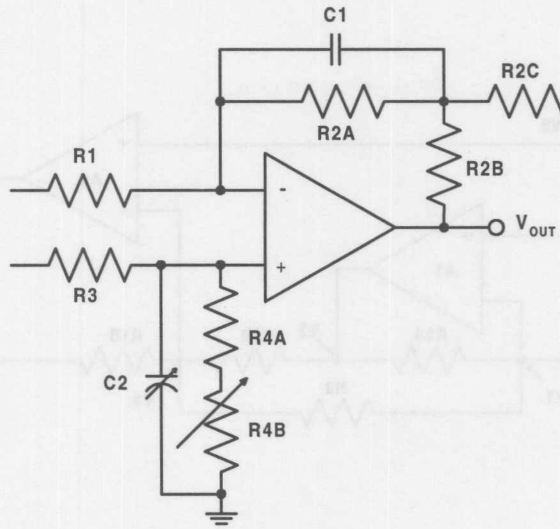
Let's look at the pros and cons of this circuit. It certainly is a minimum parts count. One amplifier and four resistors seems to be a low cost solution. Another advantage is the ability to handle very large common-mode voltages that exceed the supplies. For large voltages, such as +/- 100 Volts, the resistors must be very large to avoid significant power dissipation. The bias current will flow through the resistors and cause an additional error, but the 6 picoamps of the LMC2001 causes a negligible error. Although there are other op amps with picoamps of bias current, a difference amplifier also requires low, or no offset voltage over time and temperature.

However, if we neglect offset voltage, input bias current, etc. for the amplifier, the equation for the output voltage still consists of terms:

$$V_0 = \left(\frac{R4 \times R1 - R2 \times R3}{R1 \times R3 + R1 \times R4}\right) V_{CM} + \left(\frac{1 + \frac{R2}{R1}}{1 + \frac{R3}{R4}}\right) Vi2 - \left(\frac{R2}{R1}\right) Vi1$$

If R1:R2 = R3:R4, then the first term is zero, and the common mode gain is zero. A mismatch of only 0.1% will result in a common mode rejection ratio (CMRR) of only 60 dB.

The Difference Amp II



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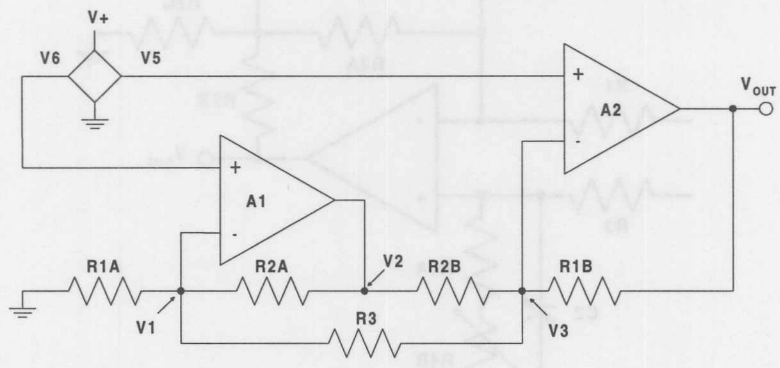
To improve the DC CMRR of the basic difference amplifier, we can make one of the resistors, (R4) adjustable. This changes the R3:R4 ratio to match the R1:R2 ratio. The DC CMRR can be improved by 20-30 db. With careful adjustment. Unfortunately, it also changes the DC gain. This can be handled by a gain adjust or full scale calibration somewhere else in the system or in software.

By adding a fixed capacitor across R2A, and an adjustable capacitor across R4, the AC impedances can be matched over a wide range of frequencies, thus improving AC CMRR by another 20-30 db. This is important to preserve gain accuracy when measuring a varying signal such as the pressure variation in an internal combustion engine.

Both of these methods would require production trimming.

If there is a microprocessor in the system, switches can be added to reverse the connections from the transducer to the difference amplifier. A subtraction can be done in software to eliminate the common mode signal, leaving twice the normal mode signal as a result.

Two Amp Instrumentation Amplifier



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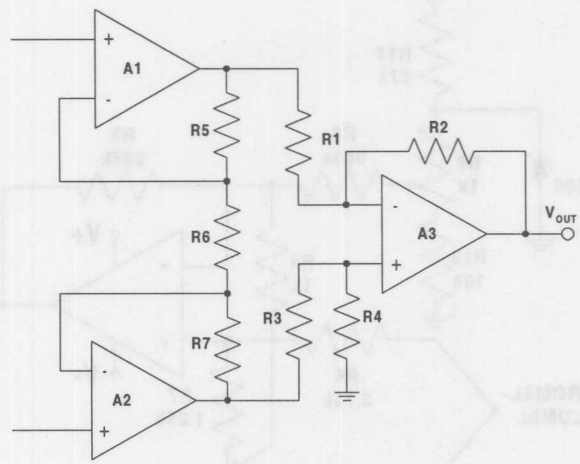
The two op amp instrumentation amplifier has a higher component count, but for the price of one op amp, we get very high input impedance on both inputs. This means that the transducer is not unequally loaded. In the "old days", this would still mean tens or hundreds of nanoamps of bias current, but today it means less than 10 picoamps. If we add one resistor, R3, we can adjust the gain without affecting the CMRR.

Note that the inverting signal path through amplifier A1 is longer than the signal path through A2. This unequal time delay will manifest itself as degraded AC CMRR.

The output of A1 is a function of the common mode signal, and the normal mode signal together. This usually limits this topology to higher gains, say greater than 10. For low gains, e.g. Av = 2, V2 may be driven to the positive rail. For higher gains, the gain of A1 is lower and approaches 1. The input voltage of the first amplifier must be less than R1A/(R1A + R2A) times the output saturation voltage.

The input capacitance of the op amp's non-inverting inputs, in conjunction with the transducer impedance, forms a low pass filter. The inputs should be guarded to reduce this effect. Although the capacitances are small, with large value resistors and high gains, the error can be sufficient to limit the accuracy to less than eight bits at 5 kHz.

The Classic Instrumentation Amplifier

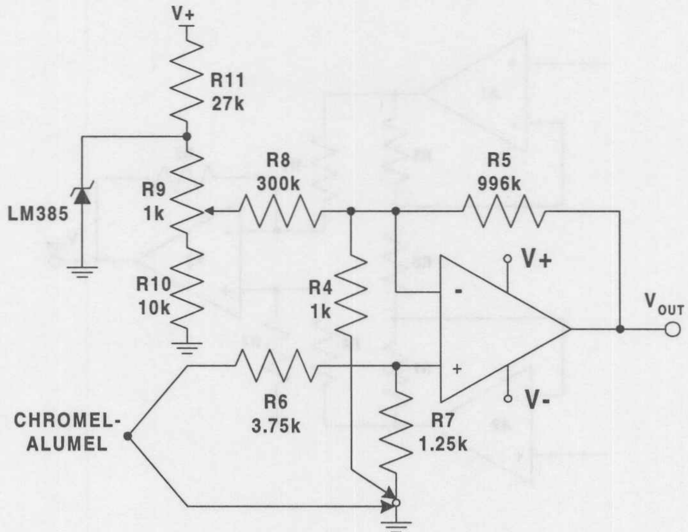


The classic three op amp instrumentation amplifier is the most well known. The back end is the difference amplifier from the previous page, and is driven by the low output impedance of op amps. Although it requires three op amps, linear parts also have improved cost/performance ratios along with microprocessors and DRAMs. Precision op amps are no longer five dollars apiece, so for the price of one op amp years ago, you now can get three and have change left over. In terms of disadvantages, this does have the input C problem and the bias current problem of the two amplifier solution. Again, guarding the inputs reduces the effect of input capacitance, and less than 10 picoamps of bias current with a 1Kohm source unbalance results in an offset error of less than 10 nanovolts.

An advantage of this configuration is that resistor mismatches between R5, R6, and R7 do not affect the CMRR, but only result in a slight gain error.

A subtle characteristic of this circuit is the the ability to reject Vos drift over temperature <u>if</u> A1 and A2 are a matched pair and drift in the same direction. If this is true, then the Vos appears as a common mode signal and is rejected by the circuit. By using chopper stabilized amplifiers for A1 and A2, they effectively appear as a matched pair that match within a few microvolts over temperature.

Thermocouple Amplifier



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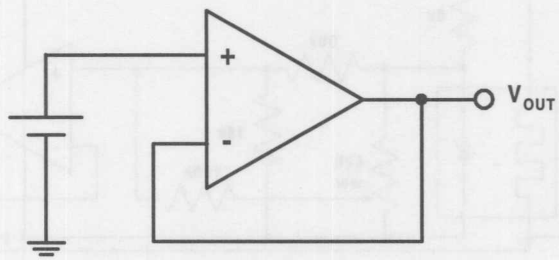
For measuring wide temperature ranges, thermocouples are quite popular due to their low cost and ease of use. Unfortunately, the output from a thermocouple is in the range of 5 microvolts per °C to 50 microvolts per °C . The simple amplifier shown takes advantage of the low offset and near zero Vos drift of the LMC2001. For best performance, resistors should be carefully chosen. Good choices are precision wirewounds, Vishay bulk metal or precision metal film types with a 1% tolerance and a temperature coefficient of +/- 5 ppm/ °C or better.In addition to having a low TCR, these resistors exhibit low thermal emf when the leads are different temperatures, in the range of 0.5 to 3 uV/ °C.

Although analog circuits have been developed that partially correct for the non-linearity, microcontrollers are so inexpensive, it makes sense to do the correction in software.

Any two metals that are different will form a thermocouple, so all junctions between resistors, solder, pc board traces, connectors, etc. should be modeled and balanced.

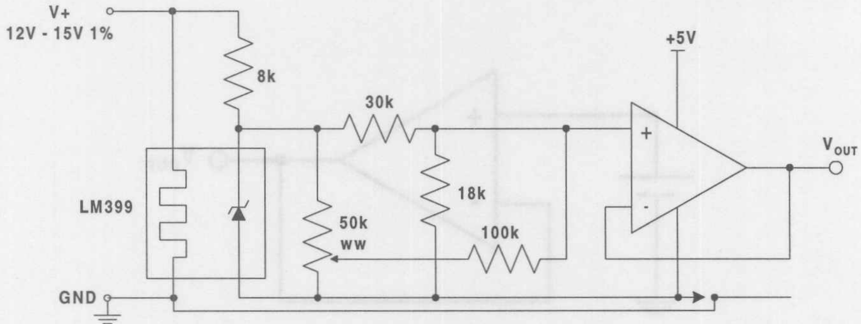
For further details, see AN-225.

Standard Cell



To create a laboratory voltage reference, a standard cell is used. If any current is drawn from the cell, its value as a reference is permanently destroyed. (By current is meant greater than 10 nanoamps.) The 6 picoamp bias current of the LMC2001 and essentially zero offset drift is a natural for this application.

Standard Cell Replacement



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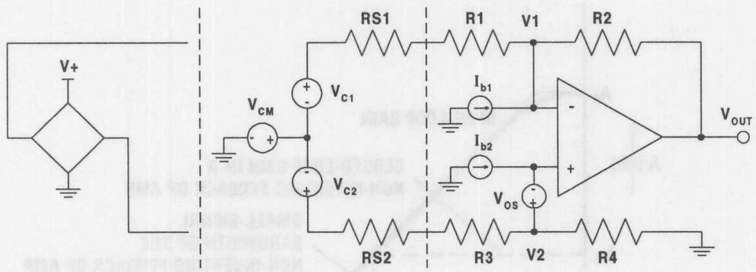
A laboratory voltage reference has traditionally been a standard cell. This cell cannot have even a momentary load, or its long term stability and calibration will be permanently degraded. A good secondary voltage reference can be made with a minimum of components very inexpensively.

The LM399 is a buried zener with an on chip heater that maintains the die temperature at 85 °C . The normal emitter base junction, when zenered, breaks down at the surface of the silicon and is therefore susceptible to surface effects. The breakdown is noisy, and cannot give long term stabilities much better than about 0.3%. Buried zeners have low noise and good long term stability. By using the LMC2001, the amplifier drift over time and temperature is eliminated. The only remaining errors come from the passive components.

Error Sources



Error sources

Vos, delta Vos (temp and time), Ibias, Ios, CMRR, PSRR, GBW/SR

Remaining error sources

transducer self heating

transducer nonlinearities

Thermocouple effect of leads, solder, connectors, sockets

Resistor thermal emf

Unequal lead lengths or foil area

Mechanical noise, e.g. variable stray capacitance from bending cables

Air currents

Resistor ratios, tempco, tracking tempco

Bias current times resistance

Line frequency pickup

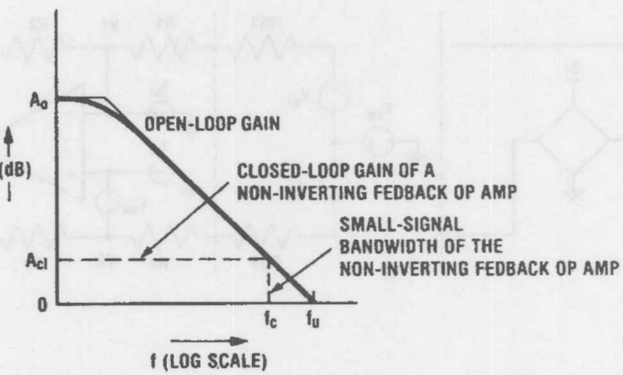
Electrical overstress, e.g. zener emitter-base junction

Ground Loops/IR drop, use Kelvin sensing

Input capacitance or stray capacitance

Reference errors

Closed-Loop Bandwidth Depends on Closed Loop Gain



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For the LMC2001, there effectively is no 1/f corner. For most applications such as temperature, we would band limit the gain stages to a low frequency, say 10 Hertz. If this is the case, why is the Gain Bandwidth (GBW) 6 MHz.? Why is the slew rate 5 V/uS? Well, other applications may require wider bandwidths and/or significant signal amplification. As an example, for monitoring the pressure variations in an internal combustion engine at 5,000 RPM, the frequency can be greater than 3 kHz.

The closed loop, small signal bandwidth of an op amp, limits the rise time, tr, that can be obtained in the output voltage waveform following a small signal step change in the input voltage. The one key equation linking the time domain to the frequency domain is that the rise time of a system with a single high frequency roll-off depends on the closed loop small signal bandwidth:

$$Tr = 0.35/F_{3db}$$

If the unity gain frequency of the op amp is Fu, after some algebraic manipulation, we get:

$$Tr = (0.35/Fu)\ Acl$$

For a closed loop gain of 100, this would result in a rise time of 5.8uS, compared with 11uS to 70uS for other stabilised amps. For large step changes at low gains, the slew rate may be the limiting factor. Again, the 5 V/uS is significantly better than the usual 0.5 to 2 V/uS of competing devices.

Another way of looking at this is to consider a gain of 100, which would result in a corner at 60 kHz. This will be -3 dB down, or a 29.3% AC error! At 0.1 Fc, the error will be -0.04 dB., which doesn't sound like much, but this is a 0.5% error using up the complete error budget for a 7 bit system. At 0.05 Fc, or 1200 Hz., the error is -0.011 db., which is a 0.125% error, or roughly half of an LSB in a 12 bit system.

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High-Speed Amplifiers

- **Smaller packages (SOT23-5)**
- **More affordable**
- **Application Solutions:**
  - low power output stage - capacitive load drive
  - high output current - low distortion
  - low noise - cable driving
- **Simulation models and application notes**

National Semiconductor

More devices are now available with space saving in mind. The complete list of National Semiconductor devices offered in SOT23-5 is shown below:

Device	Description	Supply (V)	Type	BW@Av (MHz)	S/R (V/us)	Icc (mA)	Iout (mA)
CLC109	Closed Loop Buffer	+/-3 to 13	BUF	270 @ 1	350	3.5	30
CLC404	Wideband, High Slew Rate	+/-5	CFB	175 @ 6	2600	11	70
CLC406	Wideband, Low Power	+/-5	CFB	160 @ 6	1500	5	70
CLC409	Very Wideband, Low Distortion	+/-5	CFB	350 @ 2	1200	14	70
CLC425	Adj. Icc, Ultra Low Noise, Wideband	+/-5	VFB	95 @ 20	350	15	90
CLC450	Low Power, High Output Current	+5 to +/-5	CFB	135 @ 2	370	1.6	130
CLC451	Low Power, High Output Current, PGB	+5 to +/-5	CFB	100 @ 2	350	1.6	130
CLC452	Low Power, High Output current	+5 to +/-5	CFB	160 @ 2	540	3.2	130
CLC453	Low Power, High Output Current, PGB	+5 to +/-5	PGB	130 @ 2	460	3.2	130
LM7121	Low Power, High Speed	+5 to +/-15	VFB	235 @ 1	1300	5	40
LM7131	Low Voltage, High Speed	+2.7 to +/-5	VFB	90 @ 1	130	7.5	65

Several new Programmable Gain Buffers (PGB) with various combination of features are now available. The complete list of these devices is shown below:

Device	Feature	Supply Range (V)	BW @ Av (MHz)	SR (V/us)	Icc (mA)	Iout (mA)	Vos (typ/limit) (mV)	Package
CLC451	Low Power, Hi Output, Single	5 to +/-5	100 @ 2	350	1.6	130	3/35	DIP, SO, SOT23
CLC453	Low Power, Hi Output, Single	5 to +/-5	130 @ 2	460	3.2	130	7/35	DIP, SO, SOT23
CLC5612	High Output, Dual	5 to +/-5	90 @ 2	290	1.6	130	3/35	DIP, SO
CLC5632	High Output, Dual	5 to +/-5	130 @ 2	410	3.2	130	7/35	DIP, SO
CLC5633	High Output, Triple	5 to +/-5	130 @ 2	410	3.2	130	7/35	DIP, SO

Recent devices contain low voltage characteristics tables to facilitate design into the latest battery operated and portable equipment.

As always, the devices available are backed by simulation models and application notes which provide useful information to the designers.

Low Voltage/ Low Power and High Speed Operation

- What parameters are affected at lower supply voltage
- Inherent limitation at lower supplies
- Advantages/ disadvantages of migration to lower supplies
- Latest product offerings which achieve low voltage performance using state of the art processing techniques and design methodology

While offering an efficiency improvement, operating at lower supply voltages generally presents challenges in the following areas:

1) Lower bandwidth	2) Less output current	3) Less loop gain
4) Reduced common mode range	5) Reduced slew rate	6) Increased distortion
7) Increased settling time	8) Reduced undistorted output swing	

Bandwidth, simply speaking, has an inversely proportional relationship with transistor junction capacitances. As the supply voltage is reduced, the Collector-Base junction capacitance (and substrate capacitance), which are usually the dominant parasitic in terms of BW, increase by a factor equal to 1/3 power of the ratios of its reverse bias voltage (first order approximation). Assuming that most of the supply voltage appears across the C-B junction, this means that if the supply voltage is reduced by 1/2, the realizable BW is reduced by 26%! For this reason, many high speed circuits take advantage of the reduced parasitic capacitance by operating at higher Vcc.

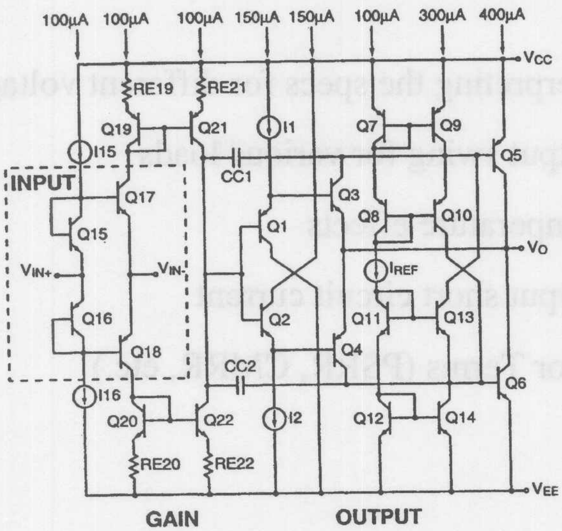
On the other hand, lower supply voltage operation offers these advantages:

1) Smaller packages- less dissipation means smaller packages with higher Thermal Resistance could be used with no compromise on reliability. Smaller packages offer the unexpected bonus of smaller geometry which in turn could translate into higher signal BW.

2) Allows the High Speed circuits to follow the general trend of lower operating voltage without the need to design in separate higher voltages for the faster portions of the design. However, the classical design approaches which dictate separate supplies for the analog/digital parts of the circuit should still be kept in mind.

Therefore, achieving high speeds while operating at lower supply voltages, has its own challenges. It is however possible to overcome some of these obstacles by utilizing innovative design methodologies and also by exploiting fabrication processes specifically designed and optimized for low voltage operation. An example of a design innovation in the output section is described in the next page.

Low Power Output Stage Delivers Exceptional Output Current and Voltage Swing



Traditionally, amplifier output stage topologies have been a compromise between having a good output swing (relative to the supplies) and being capable of delivering reasonable amount of current to the load. A new patented design approach allows output swings to within 1V of either rail while delivering in excess of 100mA (sourcing and sinking), with a quiescent current budget of only 0.8mA!

Here is a brief description of how this unique output stage achieves this:

For a positive going signal presented to Vin, the current through Q3 increases while current through Q4 decreases. This increase in Q3 current, simultaneously increases Q5 current and reduces Q4 & Q6 current (through the Q10 path) thereby increasing the net current delivered to the load.

When the output current is larger than the quiescent current of Q5, Q6 (400uA), the circuit operates as a class AB stage; that is, when the output is sourced, Q5 is the dominant active output device while Q6 becomes the dominant active device as output current is sunk.

The net effect of all this is that significant load current can be sourced/ sunk and the power consumption and voltage swing are not sacrificed to achieve this.

Several new devices (i.e. CLC5665, CLC5623, CLC5633, CLC5602, CLC5612, CLC5622, CLC5632) take advantage of this new innovative output stage design to establish a new class of High Speed, low power, and high output current devices.

It is important to note that the Vout max and Iout max specification of an Op Amp may not be simultaneous specifications. In other words, these specifications usually refer to each of the voltage and current limitations independently. When taken together, the specifications are usually more restricting because these parameters are interrelated; output current usually reduces when output voltage reaches its limit values. For an example of this, please refer to the CLC5623 output current vs output voltage plot shown later in this presentation.

When determining the output current of an Op Amp stage, in most cases the current flowing in the feedback path should be considered as well, especially for High Speed operation which generally use a low value resistor.

Low Voltage/Low Power Input/Output Specs

- Interpreting the specs for different voltages
- Output swing for various loads
- Temperature effects
- Output short circuit current
- Error Terms (PSRR, CMRR, etc.)

Input Range, Output Swing, Effective Load, and Error Terms considerations:

In the case of the CLCxxx Op Amps, the input voltage range is usually given as a single number with no signs associated with it. That is intended to mean that range is +/- the number specified (in Volts) when used with the supply voltages specified in the heading of the table. The important parameter in the common mode voltage range is the voltage difference between the appropriate supply voltage and the positive or negative common mode voltage. For example, with CLC428, the input common mode voltage range limit is +/-3.3V over temperature, when used with +/-5V supplies. If the supply voltages are reduced by 10%, the new input common mode voltage range will be +/-2.8V (or +/-1.7V from +/-4.5V).

A plot usually given in most National data sheets is the plot of output voltage swing vs output current (for either sinking or sourcing current). This plot is very useful in estimating the typical output voltage range for various loads. This is especially useful because the Electrical Characteristics tables usually only specify the output swing for a given load, which might be different than the load you need to drive.

On the subject of Error Terms, the output offset voltage for a CFB Op Amp is given by:

Output Offset Voltage Vo= +/-Ibn x Rs (1+ Rf/ Rg) +/- Vio (1+ Rf/ Rg) +/- Ibi x Rf

In CFB Op Amps, power supply, Vcc, and common mode voltage, Vcm, variations manifest themselves in changes in Vio, Ibn, and Ibi values. These variations, summed up in specs like PSRR and CMRR, reflected to the input are given by the following:

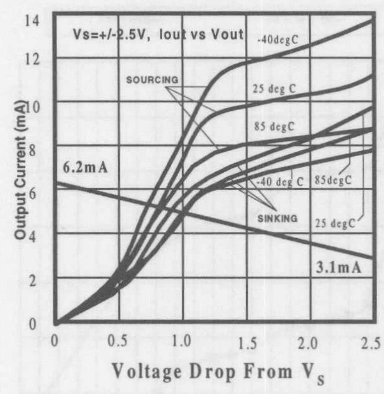
PSRR= -20x log [δVio / δVcc + δIbn x Rs/δVcc + δ Ibi x Req/δVcc]

CMRR= -20x log [δVio / δVcm + δ Ibn x Rs/ δVcm + δ Ibi x Req/δVcm]

where:

Req= Rf || Rg, and Rs= equivalent input source resistance

LM7301 Output Characteristics



Here is an example on how to estimate the output swing for a given load:

The plot of output voltage vs. output current for LM7301 is shown. Let's assume that the objective is to figure out the output voltage swing capability when this device is used in a 5V single supply application driving a 810ohm load to ground. One easy way to determine this would be to construct the load line corresponding to the load used and find the intersection of the load line with the current sourcing plot (since in this case no current sinking capability is required). The load line can be constructed by finding any two points corresponding to the load specified and then connecting a line between them. For this example, it is found that the intersection occurs at an output swing of about 0.9V from V+ (or 4.1V output) at 85°C. This point is when the Op Amp is delivering about 5mA to the load. Please note that this is a typical output swing over temperature. The limit would be less.

The equivalent closed loop load impedance (also known as Effective Load) is given below:

Non-inverting configuration: Rout= RL || (Rf + Rg)

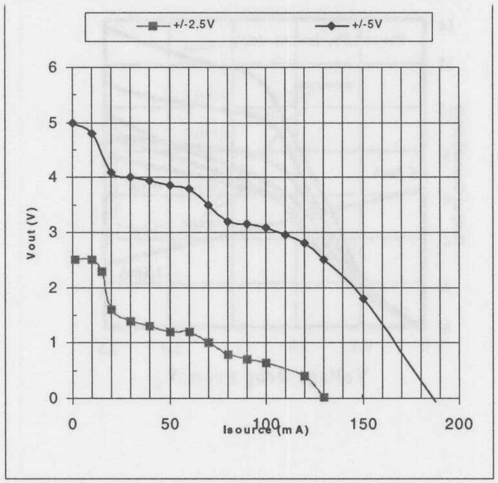
Inverting configuration : Rout= RL || Rf

Unity gain applications are limited by the CMVR. With greater non-inverting gains, Vout range becomes the limitation. For inverting applications, Vout range is the limitation as well. Obviously, for inverting (or transimpedance) applications, the following has to hold:

|Iinv| <= Vmax/ Rf

When looking at output voltage range and limits, it is important to consider the overall output load.

Another parameter usually found in all National Op Amp data sheets is the "output short circuit current". In this case, for example, the specification calls for 10.9mA sourcing typical. Looking at the Vo vs. Iout plot shown, this spec is confirmed since at 25C, the sourcing current plot is at about 11mA when "voltage drop from Vs" is at 2.5V. Short circuit current for a dual supply (or single supply) specification is the current which flows when the output is shorted to gnd (or half supply). The input is driven such that sourcing and sinking current can be determined.



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Here is an example of how reducing the supply voltages in effect reduces how much current can be delivered to the load. The example shown belongs to the CLC5623 sourcing output current when operated with +/-5V supplies and +/-2.5V supplies.

As can be seen, in either case the output swing increases to very near the supply rails with a light load. However, when the supplies are reduced from +/-5V to +/-2.5V, even though the absolute voltage and current numbers change, the output swing relative to the pertinent rail (supply) stays consistent. An example would clarify this:

Here are some data taken from the plots shown:

Supplies	Vout@Iout=50mA	Vout from V+
+/-5V	3.8V	-1.2V
+/-2.5V	1.3V	-1.2V

As can be seen from the numbers shown above (and also from the similar shape of the two plots), the third column numbers (Vout from V+) are the same.

Therefore, in most cases, if the characteristics for a set of supply voltages are known, it is possible to construct the characteristics for another set of supplies by referencing the sourcing voltages to the positive rail and the sinking voltages to the negative rail. Graphically, this means shifting the plot up or down along the vertical axis.

Distortion in High Speed Amplifiers

- What is it?
- Factors which contribute
- Different ways of representing Distortion
- Converting from one representation to another
- Distortion causes
- Intermodulation Distortion
- -1dB Compression point
- Using I2, I3, and IM3 specifications
- Reducing distortion
- Examples from recent devices and how the specs change under different operating points *(load, supply voltage, gain, etc.)*

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Harmonic Distortion of an Op Amp is determined by several factors:

Small and Large signal nonlinearity of the amplifier

Amplitude and Frequency of the test signal

Amplifier load

Power supply voltages used

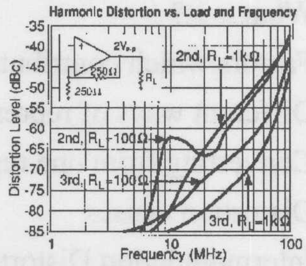
Layout, grounding, and power supply decoupling

Circuit's loop gain at the frequency of interest

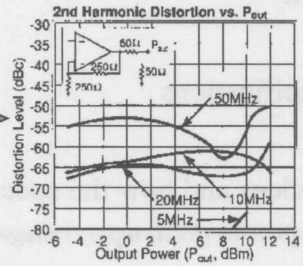
Therefore, the test conditions are very important when comparing devices and/or interpreting specs.

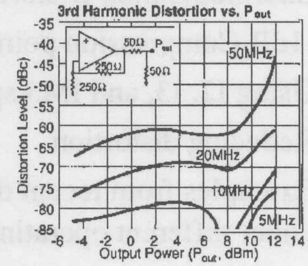
CLC409 Distortion Performance

2nd/3rd HD with RL=100Ω
and
2nd/3rd HD with RL=1kΩ



5MHz
20MHz
and
50MHz
Distortion
Performance





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Harmonic Distortion plots/ specs are done in several different ways (i.e. %THD, ppm THD, THD+N, dB, dBc, or 2nd or 3rd order intercept in dBm). THD numbers are usually dominated by the first 5 or 6 terms. Since THD is determined by Root Sum Square (RSS), the lower harmonics with their higher order terms tend to dominate. THD+N numbers include the noise at the output as another term which is included with the other RSS terms. This noise term should be integrated over the measurement bandwidth. In Audio applications, the BW is taken to be around 100KHz. It is always possible to calculate THD+N given the THD number and the amplifier's noise voltage and noise current specification over the BW of interest.

dBc specification vs frequency simply means that the THD at a given frequency is so many dB's below the "carrier" or fundamental frequency. Here is how to convert between THD numbers and dBc:

dBc= 20x log [%THD] - 40

%THD= ppmTHD x (1X104)

THD= SQRT (V22 + V32 + V42 +…. + Vn2) / Vs

THD+N= SQRT (V22 + V32 + V42+….+ Vn2 + Vnoise2) / Vs

Where Vs is the signal amplitude (rms Volts) and Vn is the nth harmonic amplitude (rms Volts)

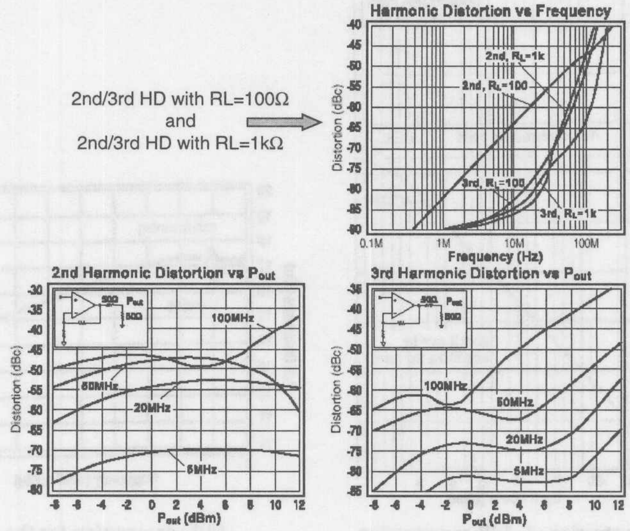
Vnoise is the rms value of noise over the measurement BW

Intermodulation distortion specification allow fair comparison between different amplifiers since the number is independent of the amplitude.

CLC449 Distortion Performance

2nd/3rd HD with RL=100Ω
and
2nd/3rd HD with RL=1kΩ

5MHz
20MHz
50MHz
and
100MHz
Distortion
Performance



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Second order harmonic distortion is rather constant for a wide range of output power levels. This is typical of a class AB output stage. The major cause for the second order distortion is the mismatch between the positive and negative paths of the complementary circuit.

Third order harmonic distortion is mostly a function of the crossover distortion which is typical of a class AB output stage. In many amplifiers, the crossover distortion actually reduces at higher output levels because at higher levels, the crossover region is a smaller percentage of the overall signal.

1dB Compression Point

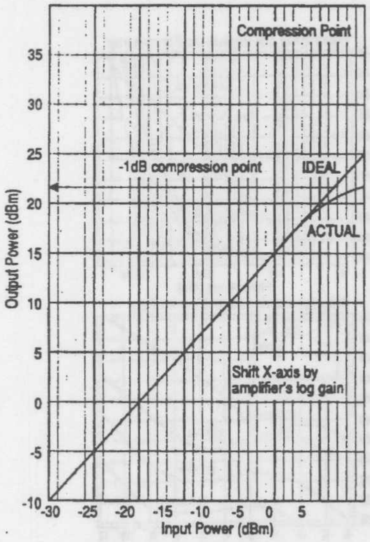
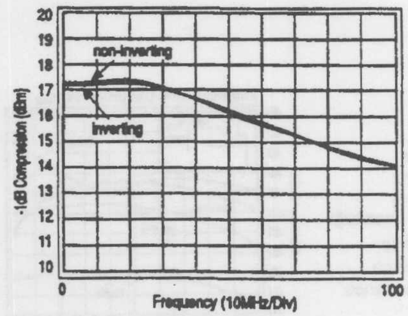


Illustration of -1dB compression



-1dB compression for the CLC404

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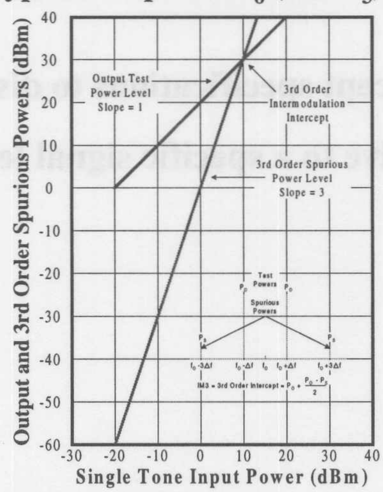
The 1dB compression point can be thought of as the end of the usable range of an amplifier. By definition, it refers to the input power (dBm) where the actual output power is 1dB below the theoretical value. From this point onward, the linear relationship between input and output power no longer holds and the amplifier has reached the end of its usable range. At low frequencies, the 1dB compression point is mainly dominated by the amplifier dynamic range but at higher and higher frequencies, slew rate limiting starts to play a role.

The 1dB compression point and harmonic distortion performance are inter-related concepts and usually by measuring one of these values, one could determine the other one by calculation.

Distortion in High Speed Amplifiers
Intermodulation Distortion

Typical Amplifier P_o (and P_3) vs P_{in}



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Harmonic Distortion

Sometimes, rather than using a single tone to test the THD of an amplifier, it is useful to look at the distortion products of two tones which are close to each other in frequency. This measurement is called Intermodulation Distortion (IMD). This is of special interest in RF and IF applications and multi-channel communication system with constant channel separation across the frequency band. It turns out these closely spaced distortions are more troublesome than the integer harmonic distortion terms that appear in increments from the main frequency.

By applying two frequencies f1 and f2 to a non-linear stage, it turns out that only the third order resultant product terms, 2f1-f2 and 2f2-f1 (or fo-δf/3 and fo+δf/3 where fo is the average frequency and δf is the separation of each tone relative to fo), are most troublesome because they would end up very close to the original two tones and hence cannot be filtered out. For this reason, usually for high frequency amplifiers, the IM3 (dBm) (also called INT3), which is the third order Intermodulation Intercept point, is specified. This spec, is the output power at which the 3rd order Spurious power is equal to the single tone output power. When plotted on a log-log scale, the output power vs input power has a slope of 1, and the Spurious power vs input power has a slope of 3. Therefore, the two plots will eventually intersect each other at an output power level called IM3. It is an extrapolated measure because usually this output level is beyond the -1dB Compression point of the amplifier and hence the output has already reached its maximum swing and can no longer increase with increasing input. IM3 is a function of frequency since the output distortion increases at higher frequencies due to reduction in the loop gain.

If the two tones used are of equal power and the output test power Po , and the spurious power, Ps , are measured at a given input test power Pt, the following can be written (all numbers in dBm):

$$Po = Pt + K1 \quad \text{and} \quad Ps = 3\,Pt + K2$$

Equating these two expressions, you get: Pin3 =(K1-K2)/2, which is the input power corresponding to IM3. From this, one will get:

$$IM3 = Po + (Po - Ps) / 2$$

Converting Intercept specifications to distortion levels relative to a specific signal level

The Intercept specifications could be used to predict the distortion at the output for a given output level and frequency. Let's assume that we are interested to find out the 2nd, 3rd, and Intermodulation products of CLC231 at 10MHz when delivering 2Vpp to a (50x2)ohm load and set for Av=+2.

Here are the specifications for CLC231:

I2= 75dBm, I3= 46dBm, IM3= 47dBm

To convert peak to peak output voltage level across the 50ohm load to dBm power numbers:

Vrms = [Vpp / 2x SQRT (2)] and P= 10x log [20x Vrms ^2]

Converting 1Vpp across 50ohm load, results in +4dBm for the output power, or:

Po= +4dBm

This results in the following:

2nd Harmonic (dBm)= S2 (dBm)= 75dBm - (75dBm- 4dBm)x2= -67dBm, or -71dBc

3rd Harmonic (dBm)= S3 (dBm) = 46dBm - (46dBm- 4dBm)x3= -80dBm, or -84dBc

Intermod. 3 (dBm)= IMD3 (dBm) = 47dBm - (47dBm- 4dBm)x3= -82dBm, or -86dBc

Or in general:

S2 (dBc) = (Po - I2) (dBc) S2 (dBm) = (2Po - I2) (dBm)

S3 (dBc) = 2x (Po- I3) (dBc) S3 (dBm) = (3Po- 2I3) (dBm)

IMD3 (dBc) = 2x (Po - IM3) (dBc) IMD3 (dBm) = (3Po - 2IM3) (dBm)

All this is valid for Po < -1dB compression levels of the amplifier in question.

Improving the Intermodulation Distortion

- Increase loop gain
- Increase the quiescent operating current
- Increasing the load impedance
- Use CFA instead of VFB whenever possible
- Use Loop Gain shaping networks (see OA-22)

Factors which improve the IM3 performance of an amplifier:

Anything which increases the loop gain of the amplifier at the frequency of interest will improve the IM3 spec.

Increase the quiescent operating current

Reduce the feedback resistor of CFB's or reduce the operating closed loop gain in VFB's

Increasing the load impedance

CFB Op Amps have an inherent topological advantage in terms of lower distortion. The forward signal path is very symmetrical with well matched NPN and PNP signal paths along with fully complementary Class AB output buffer which yield low open loop distortion which would then be reduced further by the action of the negative feedback when the loop is closed

Use Loop gain shaping networks (see OA-22)

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ANALOG SOLUTIONS
OPTIMIZING SYSTEM PERFORMANCE

High-Speed ADCs

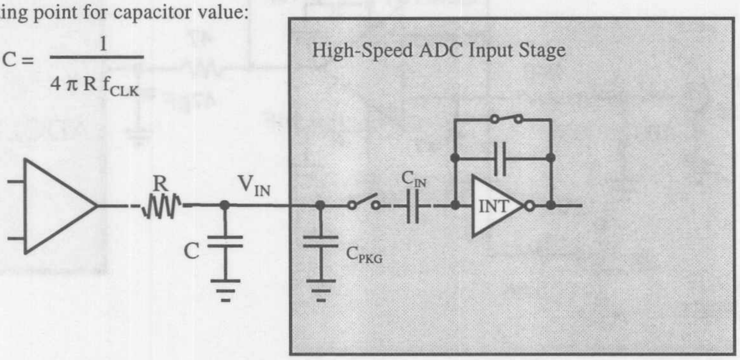
- **Driving the analog input**
  - Maintaining signal integrity
- **Voltage reference drive circuits**
- **Circuit board layout and component placement**
- **Recommended ADCs**

Driving the Analog Input

The Analog Input of a high-speed ADC is also an <u>Output</u>!

Starting point for capacitor value:

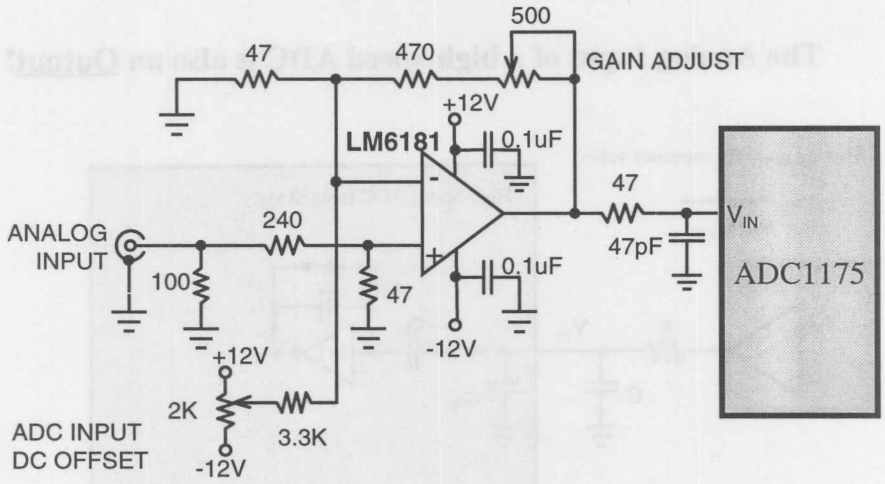
$$C = \frac{1}{4 \pi R f_{CLK}}$$



Today's high-speed ADCs have sampling switches connected to their analog input pins. The transients generated when these switches open and close can disturb the output of the amplifier driving the input pin. This in turn causes unwanted signals at the input as the amplifier's feedback loop attempts to counteract the transients. An RC between the driving amplifier and the reference inputs will isolate the amplifier from the switching transients and improve input signal fidelity. The resistor should be large enough to isolate the amplifier from the ADC input, but the RC time constant should be low enough to allow the highest input frequencies to pass without significant attenuation.

The required time constant for R and C depends upon the characteristics of the chosen op-amp, the ADC and your layout. A rule of thumb for determining the the values of R and C is to chose R = 47 to 100 Ohms, then start with a value for C according to the formula indicated here. Then measure SNR and THD. Decrease the value of C until SNR and THD are approximately equal (within 2 to 3dB of each other).

ADC1175 Input Amplifier Circuit



This is the input circuit of our ADC1175 evaluation board. The resistor and capacitor at the ADC1175 input are selected as explained on the previous page.

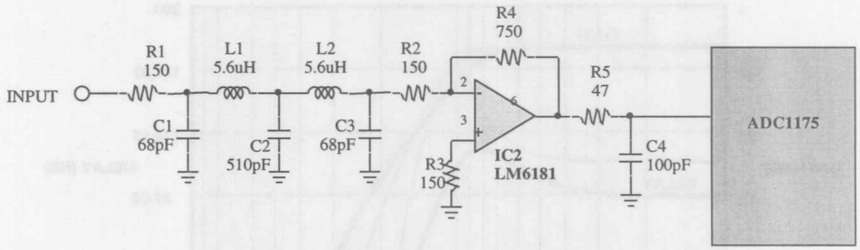
The phase margin of an amplifier at unity gain can start to become marginal, causing the amplifier output to ring a little after a high slew rate step input. The phase margin is much better at gains greater than unity. The input is divided with the 240- and 47-Ohm resistors so that the amplifier can operate at a relatively high gain to avoid phase margin problems.

The amplifier's positive supply voltage should be large enough to prevent headroom problems (+5V is sufficient). The negative supply simply needs to be at least 2V below ground to allow the amplifier to drive the ADC's input pin to its minimum voltage of 0.6V.

The 100-Ohm input resistor in parallel with the 240- and 47-Ohm resistors provide a 75-Ohm input impedance. Changing the 100 Ohm resistor to 62 Ohms will provide a 50-Ohm input impedance.

The gain and offset adjustments allow for flexibility in evaluating the converter and could be replaced in a final design solution. However, you should remember that eliminating these adjustments means that there is no compensation for tolerances and the input signal amplitude should be reduced below the full scale swing to avoid possible signal clipping.

A "Non-Standard" Input Filter



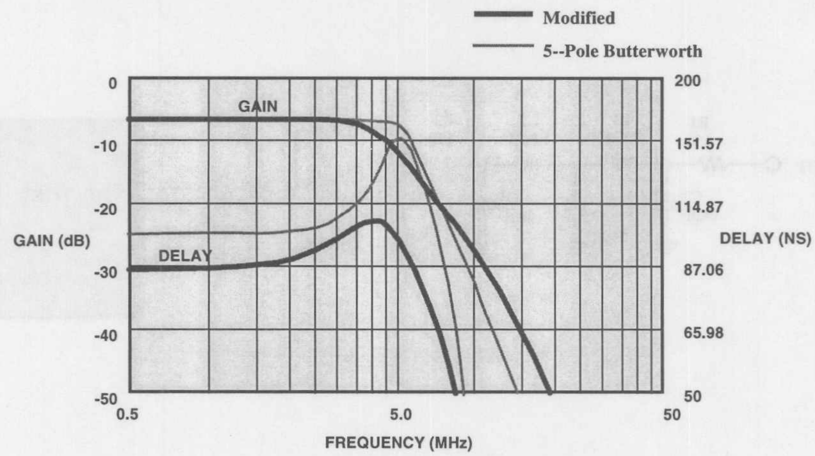
Filters are often placed in the signal path ahead of an ADC's analog input. Their most common functions are either noise reduction or anti-aliasing. Conventional filter characteristics (Butterworth, Chebyshev, Bessel, etc.) are optimized to meet very specific performance requirements, such as maximal passband flatness, but don't always behave adequately in real applications. An anti-aliasing filter for a video ADC must have a very flat amplitude response in the passband, but an "ideal" Butterworth filter will exhibit far too much variation in group delay for signals in the passband.

This is a five-pole, 4MHz low-pass filter with a Butterworth-like amplitude response and modified phase response to improve transient behavior. Capacitors C1 and C3 are reduced to 12% to 15% of the Butterworth values to achieve the improved phase response. This results in a more gentle roll-off in the amplitude response, which is rarely a problem in systems where the filter cutoff frequency is 1/4 of the sample rate or less. R1 and R2 are termination resistors for the filter. It is assumed that the source impedance is zero. For proper performance, the sum of the source impedance and R1 should be 150 ohms.

As mentioned earlier, R5 and C4 help isolate the amplifier's output from transients at the ADC's input, and also add a small phase lag that improves the phase margin of the video driver.

A plot of the amplitude and phase response of this filter is shown on the next page.

The Improved Anti-Aliasing Filter



The filter design on the previous page has a "nearly-Butterworth" amplitude response, but only a fraction of the group delay of a Butterworth filter. The lower group delay is easily recognizable as reduced high-frequency ringing after fast signal transitions.

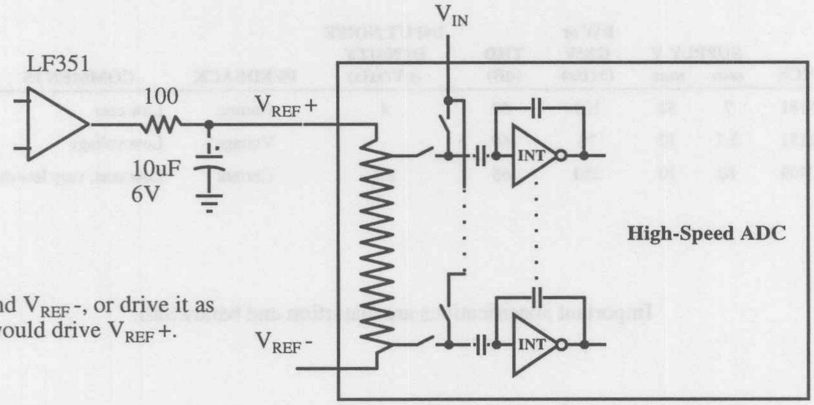
Recommended Amplifiers for Driving High-Speed ADCs

DEVICE	SUPPLY V min	SUPPLY V max	BW or GBW (MHz)	THD (dB)	INPUT NOISE DENSITY ($nV/\sqrt{Hz}$)	FEEDBACK	COMMENTS
LM6181	7	32	100	-50	4	Current	Low cost
LM7131	2.7	12	70	-60	-	Voltage	Low voltage
CLC409	10	10	350	-65	2.2	Current	Low cost, very low distortion

Important specifications are distortion and bandwidth.

Choosing the right amplifier to drive high speed ADCs is as important as any other circuit consideration when it comes to maximizing performance. The amplifier must be able to drive the dynamic capacitance of the ADC input and be able to drive a low impedance. The amplifiers listed here will give you excellent results in most high-speed data acquisition applications.

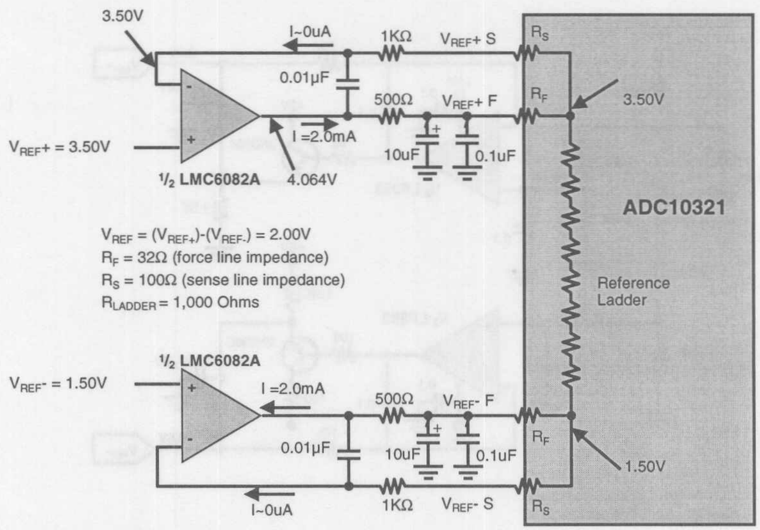
Driving the Reference Inputs of High-Speed ADCs



Ground $V_{REF}-$, or drive it as you would drive $V_{REF}+$.

High speed ADCs usually have sampling switches connected to the reference input pins. The transients generated by these switches can disturb the output of an amplifier driving the reference pin. As with the signal inputs, this causes unwanted signals at the reference input as the amplifier's feedback loop attempts to counteract the transients. Again, an RC between the driving amplifier and the reference inputs will isolate the amplifier from the switching transients and keep the reference input voltages stable. However, the resistance between the reference inputs is low enough (usually less than 1k ohm) that excessive voltage drop will occur across the output resistor, which in turn causes errors in the reference voltage seen by the ADC. This problem can be overcome by closing the feedback loop around the output resistor as done on the next page.

Reference Input Force and Sense Pins



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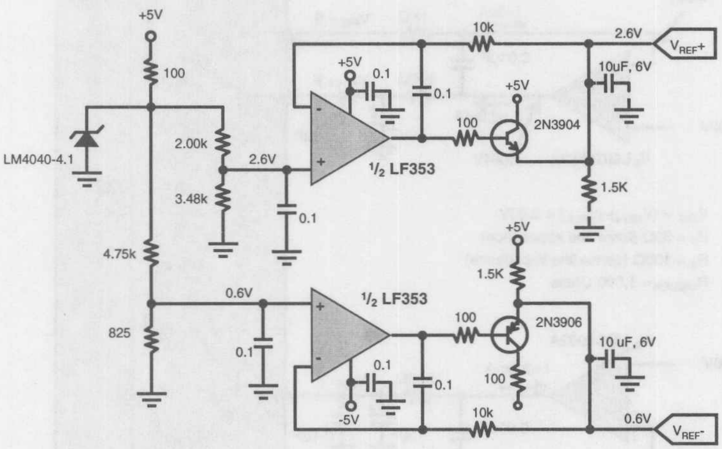
The ADC10321's force and sense pins provide a Kelvin connection capability that can be used to force the reference ladder voltage to the precise value desired by enclosing it within the amplifier's feedback loop. This eliminates errors due to voltage drops across PCB traces, bond wires, and metal/poly runs inside the device. This technique allows us to provide the ADC10321 with a maximum full-scale error over temperature that is much tighter than would otherwise be possible.

The bypass capacitors at the force inputs are required to keep the reference quiet during operation, as discussed earlier. The remaining external resistors and compensation capacitors keep the LMC6082A stable while driving this 10uF load. The LMC6082A was chosen for its low offset voltage over temperature (1mV max) and reasonable price. Amplifiers with offsets greater than 1mV or 2mV will introduce more errors than they will eliminate.

Low-Impedance Reference Driver



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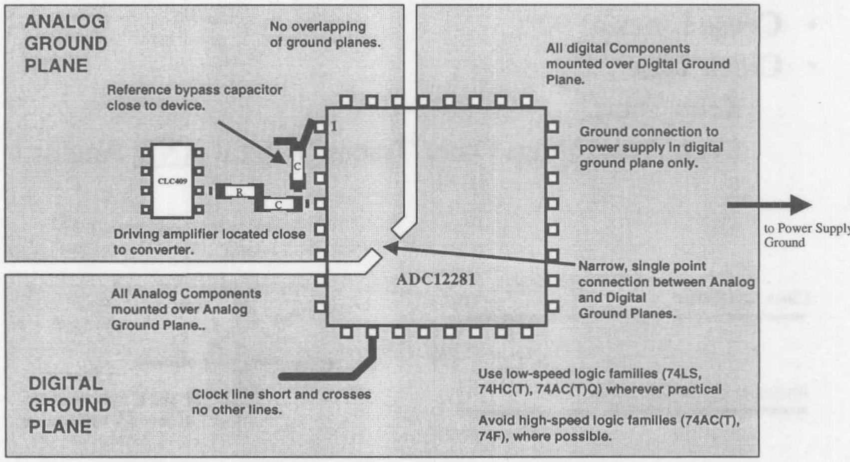
This reference driver circuit can work with ADCs that have no force and sense inputs. It avoids the use of an output RC network by adding a low-impedance buffer to the amplifier output and closing the overall feedback loop around the buffer. To ensure stability, high frequency gain is killed with a 0.1uF capacitor in each op-amp feedback loop. The transistors are connected as emitter followers, providing current gain (needed for the load), but no voltage gain (better stability). The reference voltages chosen here are those needed for the ADC1175 ADC family, including the ADC1175-50. The resistor values will need to be modified to accommodate the ADC1173, which operates with lower reference voltages. Using a relatively slow amplifier reduces the amount of noise coupled into the reference inputs.

High-Speed Layout Considerations: Analog and Digital Ground Planes



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Since the skin effect confines most high-frequency current flow to the surface of a conductor, total ground plane copper weight will have little effect on logic-generated noise. Total surface area is more important than total ground plane volume.

High-speed ADCs usually have separate analog and digital ground pins to minimize on-chip noise, but at the board level the analog and digital grounds of the A/D should be at the same potential. Connect the analog and digital grounds of the board together at the ADC and only at that point to minimize the effects of ground noise on the ADC.

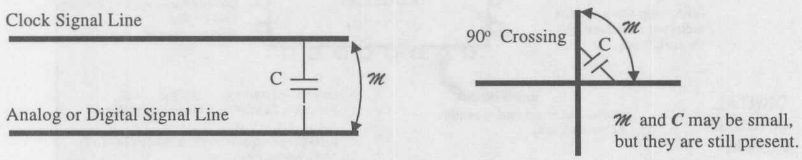
The analog and digital ground planes may be in the same layer, but should be separated from each other and, if in separate layers, should never overlap each other. With most high-speed ADCs, ground noise can be controlled by connecting the analog and digital ground planes beneath the ADC with copper that is very narrow compared with the rest of the ground plane. This narrow current path increases the impedance seen by transient digital currents, directing them away from the analog pins. The lower-bandwidth analog ground currents do not create a significant voltage variation across the impedance of this narrow ground connection. Because the analog energy can flow through this connection more easily than can the digital energy, the power ground should be connected to the digital ground plane, as close as possible to the point where the two ground plans connect.

Coupling between the noisy digital ground plane and analog circuitry can degrade noise performance. Keep the analog and digital circuitry well separated from each other and the digital ground plane. Place analog and digital components over their respective ground planes. Use power traces rather than power planes in analog areas to reduce magnetic coupling of a.c. ground currents to the power supply.

Digital circuits nearly always contribute much more supply and ground noise than do analog circuits, so choose logic devices that inject the smallest possible transients onto the ground plane. The best logic family to use in systems with A/D converters is one that employs non-saturating transistor designs, or has low noise characteristics. Worst noise generators are logic families that draw supply current during clock or signal edges. Slower logic families will produce less high frequency noise.

Isolating Signal Lines

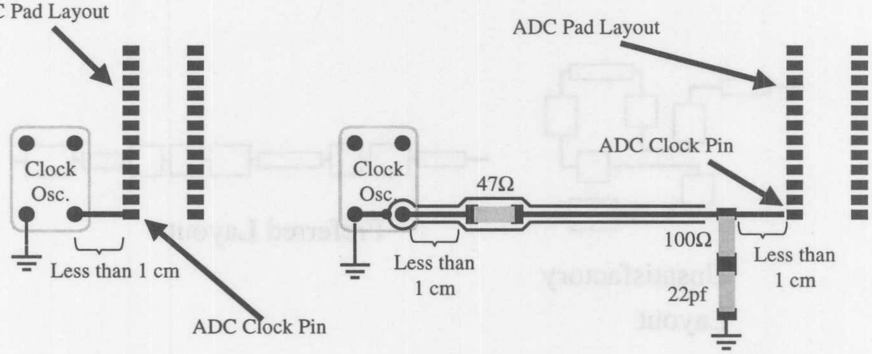
- **Cross Lines at 90°**
- **Clock Line**
  - Keep Short
  - Keep Away From Other Traces (Digital <u>AND</u> Analog)



To minimize coupling between traces, analog and digital traces should be separated. Conventional wisdom states that, when they must cross, analog and digital lines should cross each other at 90 degrees to avoid getting digital noise into the analog path. To maximize accuracy in high resolution systems, or in high frequency systems, however, we should completely avoid crossing analog and digital lines. Furthermore, it is important to keep any clock lines isolated from ALL other lines, including other digital lines. Even the generally-accepted 90 degree crossing should be avoided in such systems as even a little coupling can cause problems at high frequencies or high resolutions.

The problem with the clock line is that other, non synchronous digital signals can corrupt the clock by causing effective clock jitter, which can lead to variations in the sampling interval, resulting in poor signal-to-noise ratio (SNR).

The Clock Trace



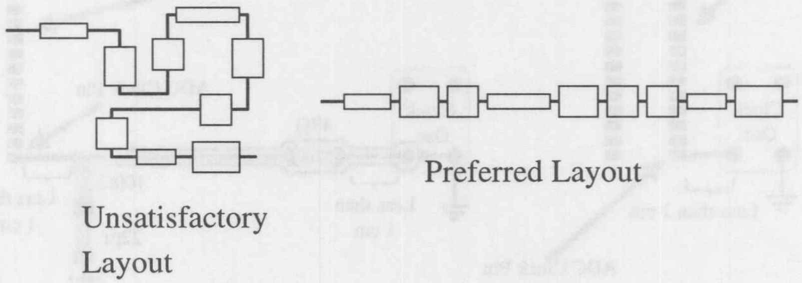
National Semiconductor   *Analog Solutions* 13

Proper design of clock traces will help to minimize reflections (which degrade SNR much the same way jitter does) as well as clock signal RFI. Clock lines that run less than 1cm in length can be treated as a simple trace. For greater clock line lengths, the trace becomes a transmission line and must be properly terminated. If it is not terminated, ringing will appear on the clock line, which will alter the effective clock timing and degrade SNR.

The 47-Ohm resistor in series with the line, combined with the clock oscillator output impedance, will equal the approximately 100-Ohm clock line impedance. This resistor should be placed as close to the clock oscillator pin as possible. The clock line is terminated within 1 cm of the ADC clock pin with a 100-Ohm resistor. The termination should always incorporate the use of the capacitor indicated to prevent dc loading of the clock source. Such dc loading could lower the amplitude of the clock signal. Again, the value of the capacitor may have to be adjusted to compensate for particular ADC type used and for the board layout.

Clock lines longer than about 1cm should have grounded “guards” to control the line impedance and to minimize RFI.

High Frequency Layout Considerations: Keep the Analog Path Straight



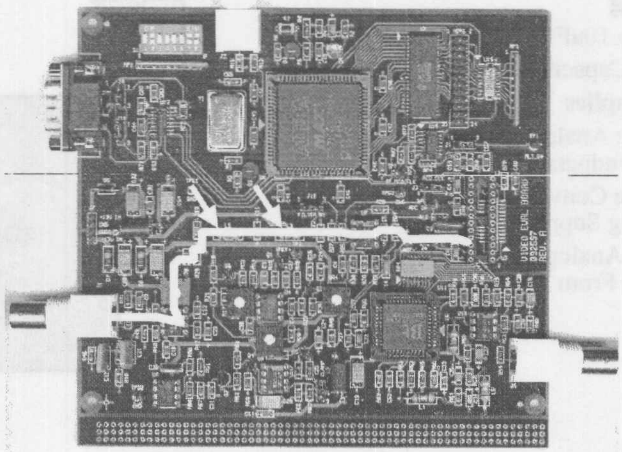
Best performance at high frequencies is obtained with a straight signal path. If the signal path folds back upon itself, capacitive and inductive coupling from one part of the circuit to another can occur, leading to unpredictable performance and increased distortion and noise. The effect is more pronounced at higher frequencies.

Be especially careful with layout of inductors. Mutual inductance can change the characteristics of the circuit in which they are used.

Here we see some possible layouts for the inductors of a filter. A filter with the inductor layout on the left would not give the same performance as a filter of the inductor with layouts on the right, because of coupling between adjacent inductors. Separating the inductors by as much distance as practical helps to reduce mutual inductance. When the analog signal path must bend, make sure that components stay separated enough to prevent interaction.

Remember that inductors are not resistors. They may LOOK like resistors, but they can not be treated like resistors when it comes to layout.

Maintain a Straight Analog Signal Path



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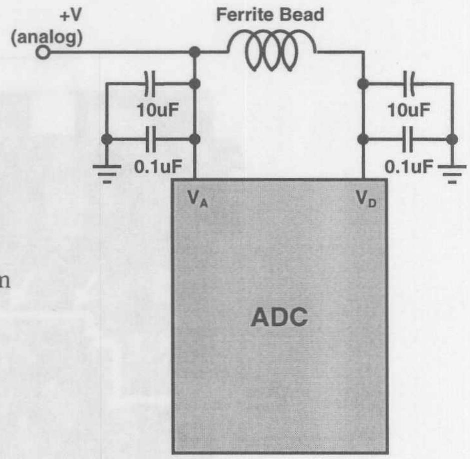
The straighter the analog signal path, the lower the chances for unwanted feedback and signal degradation. The line here show the signal path from the board input on the left to the ADC at the right side of the board. Arrows indicate the locations of inductors.

Bypassing and Supplies

- **Bypassing**
  - 5uF to 10uF Each Feed, Each Board
  - Chip Capacitors
- **ADC Supplies**
  - Isolate Analog & Digital Supplies With Inductance
  - Derive Converter Digital Supply from Analog Supply
  - Keep Analog Circuitry and Signals Away From Digital Supplies



Many A/D converters draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A 0.1uF ceramic chip capacitors placed within 2 centimeters of the A/D power pins, with a 5uF to 10uF tantalum or electrolytic capacitor should be placed as close as possible to each of the converter's power supply pins. Unleaded chip capacitors have lower lead inductance than do their leaded counterparts, so are preferred especially for the 0.1uF capacitor.

High frequency Power Supply Rejection Ratio of all analog ICs should be assumed to be zero. Data sheet PSRR specifications show good d.c. performance but rarely show a.c. performance. The a.c. PSRR is always significantly poorer than is d.c. PSRR. The analog and digital supplies of A/D converters should be well isolated from each other to prevent any digital noise from being coupled to the analog power pins. For A/D converters with very low power consumption, it might be sufficient to place a 10-Ohm to 47-Ohm resistor between the two supply lines. With an A/D that consumes a lot of power, a ferrite bead might be used in place of this resistor to avoid the associated voltage drop.

Connecting the converter's digital and analog supply pins will also help to avoid possible power supply sequencing problems.

All analog circuitry should be kept away from digital circuitry and the digital ground plane.

New 8- and 10-bit High-Speed ADCs

ADC1175
Improved Industry Standard 8-Bit ADC

- 7.2 ENOBs min at Nyquist with 10Mhz input and 20Mhz clock
- 0.35LSB typical DNL
- Best Nyquist sampling performance of any “1175” converter
- First member of pin-compatible 1175 family
- Only “1175” available in TSSOP!
- Lowest power on the market: 55mW typ, 85mW max
- ADC1175-50 is a 50MSPS version in same package/pinout

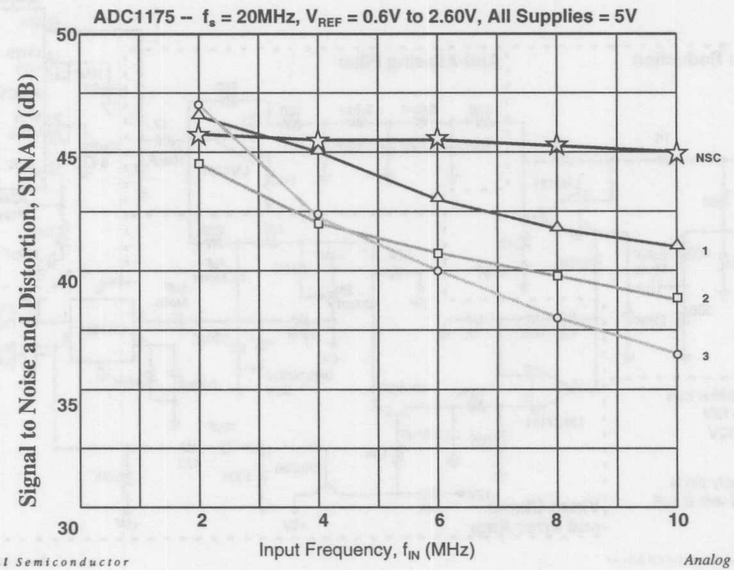
National Semiconductor

Analog Solutions 18

The ADC1175 is National’s improved version of the industry-standard 20MSPS, 8-bit ADC. It has the best “1175” ac performance and the lowest power consumption in the industry . It will drop into any “1175” socket and give improved performance, especially at higher input frequencies, as is shown on the next page. The ADC1175 also performs well at 30MSPS. For applications requiring the smallest package, the ADC1175 is the only solution in the TSSOP.

One of our sequels to the ADC1175 is a speed upgrade, the ADC1175-50, which has a 50MSPS sampling rate and is available in the same packages and pin configurations.

ADC1175 Superior Performance

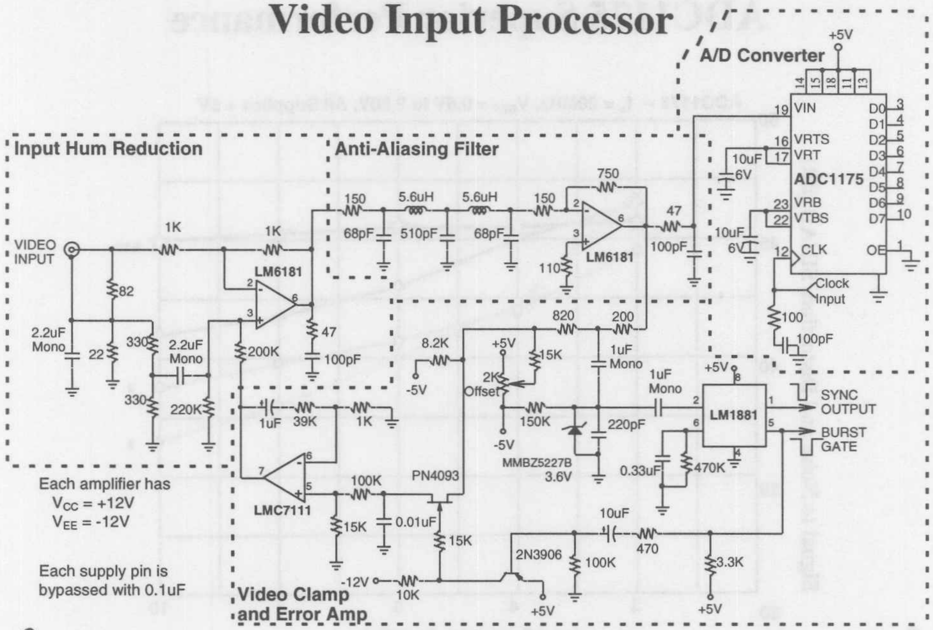


National Semiconductor

Analog Solutions 19

National's ADC1175 maintains SINAD over input frequency better than any other "1175" product. Most of National's high speed ADCs offer flat SINAD performance far beyond the half clock frequency point.

Video Input Processor



National Semiconductor | *Analog Solutions* 20

This is a very compact video input circuit with input clamp and hum rejection. Note that it uses the same low-pass filter we discussed earlier. There is no reference driver circuit. Instead, the reference is derived from the power supply by the ADC1175 with its "self-bias" configuration. This is acceptable because the input offset and gain are both adjustable.

Note that the video input is ground-referenced for high frequency ac, but not for dc and low frequencies. These is done to allow the input signal to be presented to fhe first amplifier as a differential signal as far as low frequencies are concerned, providing about 30dB of common-mode hum and noise rejection.

The clamp circuit departs from the norm in that it is dc-coupled, allowing very low frequencies to pass without attenuation and also eliminating the need for very large coupling capacitors. The clamping action is accomplished by servoing the dc level of the signal to that desired by the input of the ADC. For composite video signals, the two transistors conduct during the burst interval to charge the capacitor at the non-inverting input of the LMC7111 to a level determined by the signal's dc level and the setting of the Offset potentiometer. The LMC7111 is configured as an integrator that averages the dc value over many samples. In the absence of composite video, the two transistors are constantly conducting and the video input to the ADC remains within the expected input range of the ADC.

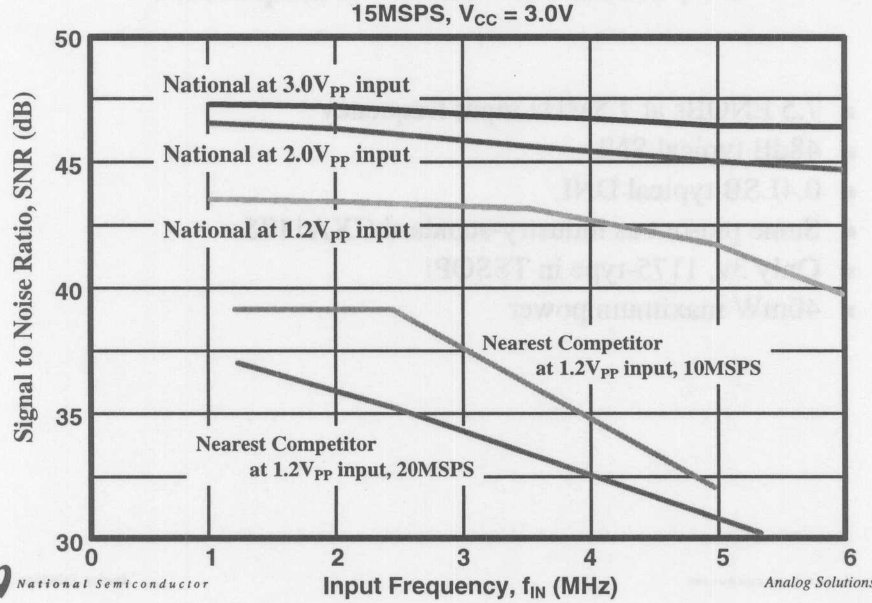
ADC1173
3V, 15MSPS "1175"-Compatible

- 7.5 ENOBs at 7.5MHz input frequency
- 48dB typical SNL
- 0.4LSB typical DNL
- Same pin-out as industry-standard CXA1175
- Only 3v, 1175-type in TSSOP!
- 40mW maximum power

National Semiconductor

The ADC1173 provides nearly the performance of the ADC1175, but on a +3V supply, making it ideal for low-power, portable applications. It is available in both the industry-standard 24-lead SO package and the TSSOP.

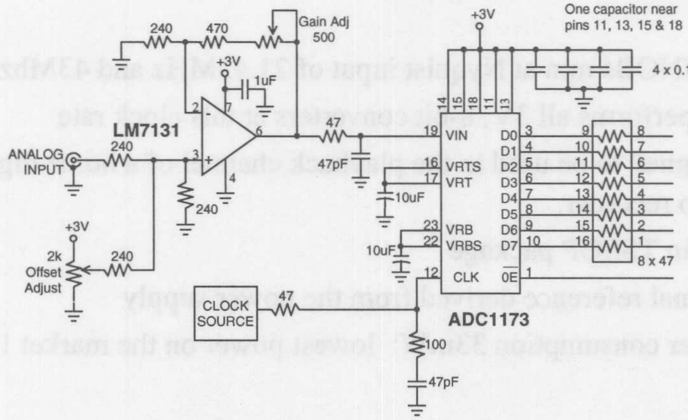
ADC1173: Superior Performance



National Semiconductor Analog Solutions 22

Like our ADC1175, the ADC1173 maintains SNR and SINAD performance over input frequency better than competitive products. Here we compare SNR rather than SINAD because the competition the does not indicate SINAD performance on the data sheet.

ADC1173 Imaging Front End



This is a high-speed, low-cost, image digitizer that operates on a single +3V supply. It is ideal for battery-powered applications such as digital cameras. The LM7131 low-voltage, high-speed amplifier conditions the input signal for the ADC1173. Note that no reference drive circuit is used in this example. Instead, the ADC1173 develops its own reference from the power supply. A little dc accuracy is sacrificed, but many high-speed applications are tolerant of moderate dc errors.

The offset and gain adjustment potentiometers on the input stage are intended for initial development use and will normally be replaced with fixed resistors in a production system.

ADC08351
3 V, 8-Bit, 42MSPS ADC

- 7.2 ENOBs min at Nyquist input of 21.45MHz and 43Mhz clock
- Out performs all 3V, 8-bit converters at this clock rate
- Designed to be used in the playback channel of a home digital video recorder.
- 20-pin TSSOP package
- Internal reference derived from the power supply
- Power consumption 33mW: lowest power on the market !

National Semiconductor Analog Solutions 24

The ADC 08351 is designed for digital data recovery in high-speed systems with ac-coupled digital signals. This includes set top boxes, cable modems, web boxes, digital camcorders, and DVD players.

This is the lowest-power ADC of its type on the market. Its 3V operation and compact, 20-pin TSSOP package are major advantages in portable systems.

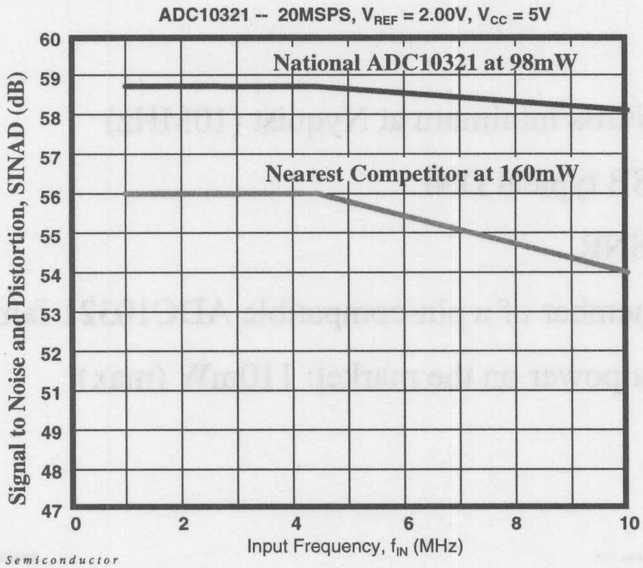
ADC10321
10-Bit, Low-Power, 20MSPS ADC

- 9.2 ENOBs minimum at Nyquist (10MHz)
- 0.35LSB typical DNL
- 58dB SNR
- First member of a pin-compatible ADC10321 family
- Lowest power on the market: 110mW (max)

National Semiconductor

The ADC10321 combines excellent ac and dc performance with the lowest power consumption on the market. It is the first of a series of pin-compatible ADCs (we also have a 15MSPS pin-compatible device called the ADC10221).

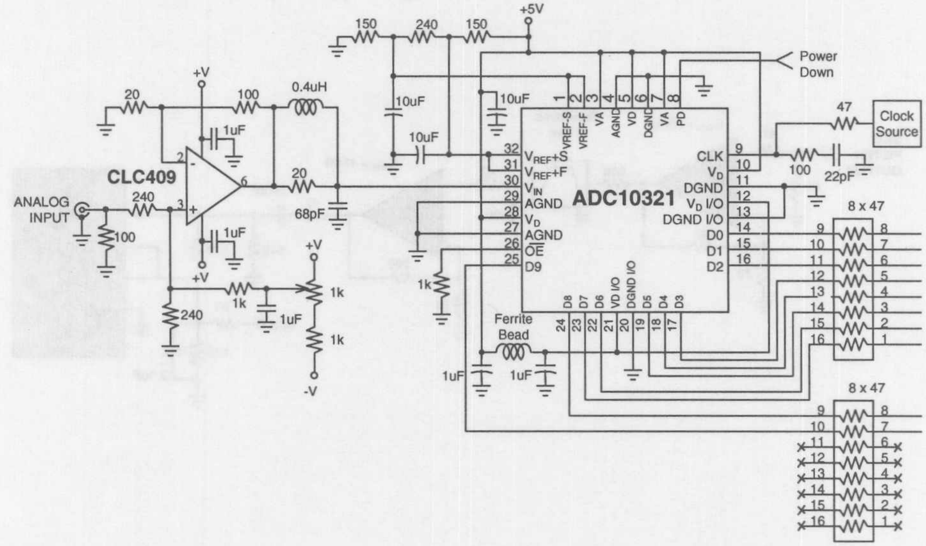
ADC10321: Superior Performance



National Semiconductor — Analog Solutions 26

In addition to the lowest power on the market, the ADC10321 superior performance. Note how its SINAD performance is maintained as input frequency increases.

ADC10321 Signal Conditioning



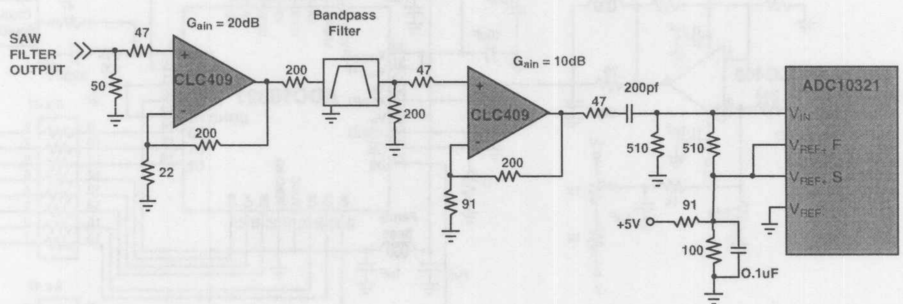
National Semiconductor

Analog Solutions 27

This shows basic circuitry needed to condition an input signal for the ADC10321. As with a couple of earlier examples, the reference voltage is derived from the power supply. If better reference accuracy is needed, the force and sense reference driver shown earlier will provide excellent performance.

Note the resistors at the digital output pins. These reduce edge rates to minimize noise and provide impedance conversion for long traces.

ADC10321 IF Sampling Circuit



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In this IF sampling circuit, the ADC10321 is used to downconvert IF directly to baseband digital. In a cable modem, for example, the IF might be at 45MHz, with a 6MHz bandwidth. Sampling at a 6MHz rate produces baseband data, but only if the input of the ADC allows precision conversions at high speeds, as the ADC10321 does. This technique reduces cost and board space while improving the quality of the resulting data.

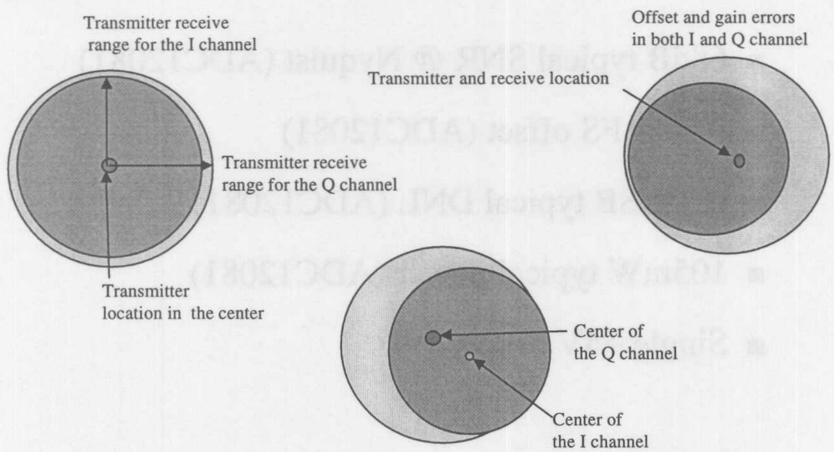
ADC12081, ADC12181, and ADC12281 12-bit, 5, 10, and 20MSPS ADCs

- 68dB typical SNR @ Nyquist (ADC12081)
- 0.05% FS offset (ADC12081)
- 0.35LSB typical DNL (ADC12081)
- 105mW typical power (ADC12081)
- Single +5V supply

National Semiconductor

The “ADC12X81” family of 12-bit ADCs has high performance at low power and sampling rates from 5MSPS to 20MSPS. All three of these converters uses self-calibration to minimize linearity, offset, and gain errors under all conditions..

When Do You Need DC Accuracy in a High-Speed ADC? Here's an Example:



National Semiconductor

Analog Solutions 30

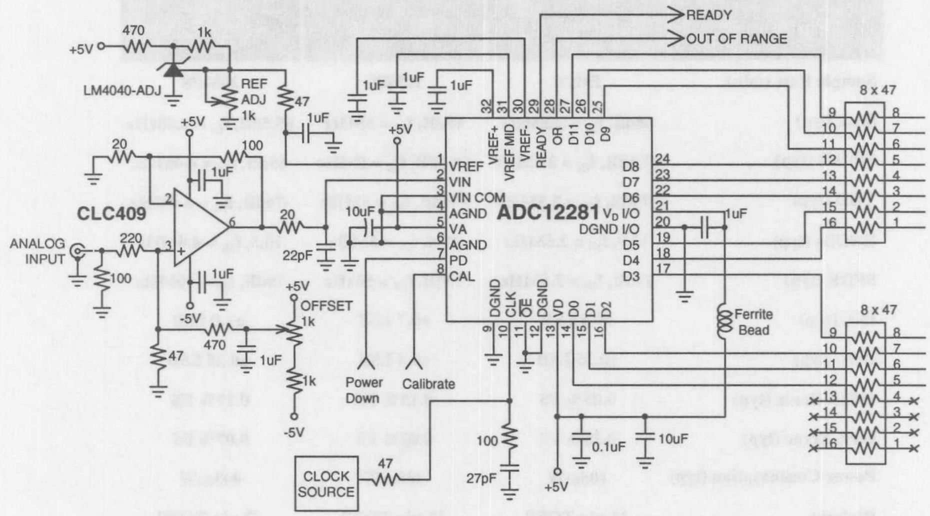
A wireless local loop uses fast ADCs to digitize the I and Q channels before sending the data to the DSP. These circles represent the operating range under various conditions. For wireless local loop the range is typically about a mile.

The set of circles on the left shows a system that has been adjusted to good offset and gain values and therefore achieves nominal range performance. The gain of the I channel is reduced for clarity so that the Q channel is visible.

The second set of circles shows the effect of gain and offset errors in the I channel on the receive side of the transceiver. The effective center of the range moves due to offset in the ADC, and the maximum range is reduced by gain errors. If the offset or gain drift with temperature, the circles will move around.

ADC that have large gain errors or offset errors will give undefined coverage. The ADC12X81 series has self-calibration to minimize offset and gain errors, and maximize performance in applications that require better precision than typical high-speed ADCs.

A 12bit 20Mhz Converter Circuit



This is a general-purpose, fast 12-bit digitizer. The input offset voltage adjustment potentiometer is used to adjust the middle of the input voltage range to 2V. If the characteristics of the input signal are known, it can be replaced with fixed resistors. Similarly, the reference voltage adjustment will typically be replaced by a fixed voltage in most systems.

In some systems the calibration function will be controlled by a microprocessor. Calibration should be performed only when the output isn't being used.

In an I and Q receiver, two of these circuits would be used, with their calibration control pins connected together for simultaneous calibration. Their clock signals should be shifted 90 degrees from each other. Dividing the system clock by four provides a simple way of getting 90 degree phase shifted clocks for a 64 Quam decoder.

12-Bit, 5/10/20MSPS ADCs

Parameter	ADC12081	ADC12181	ADC12281
Sample Rate (min)	**5MPS**	**10MPS**	**20MPS**
SNR (typ)	**68dB, f_{IN} = 2.5MHz**	**65dB, f_{IN} = 5MHz**	**65.5dB, f_{IN} = 4.4MHz**
SINAD (typ)	**67.6dB, f_{IN} = 2.5MHz**	**64.5dB, f_{IN} = 5MHz**	**65dB, f_{IN} = 4.4MHz**
THD (typ)	**-79dB, f_{IN} = 2.5MHz**	**-74dB, f_{IN} = 5MHz**	**-76dB, f_{IN} = 4.4MHz**
ENOBs (typ)	**10.9, f_{IN} = 2.5MHz**	**10.4, f_{IN} = 5MHz**	**10.5, f_{IN} = 4.4MHz**
SFDR (typ)	**79dB, f_{IN} = 2.5MHz**	**73dB, f_{IN} = 5MHz**	**75dB, f_{IN} = 10MHz**
INL (typ)	**±0.6 LSB**	**±0.7 LSB**	**±1.0 LSB**
DNL (typ)	**±0.35 LSB**	**±0.4 LSB**	**±0.35 LSB**
Offset Error (typ)	**0.05% FS**	**0.15% FS**	**0.17% FS**
Gain Error (typ)	**0.15% FS**	**0.05% FS**	**0.07% FS**
Power Consumption (typ)	**105mW**	**235mW**	**443mW**
Package	**32-pin TQFP**	**32-pin TQFP**	**32-pin TQFP**

National Semiconductor *Analog Solutions* 32

These products are leaders on dc performance (INL, DNL, gain error, offset error) and price. The low offset error means a low residual for things like demodulators for I/Q encoded signals.

Since these products all have the same pin configurations, you have an easy upgrade path from the lower to the higher speed devices.

14- and 16-Bit Converters

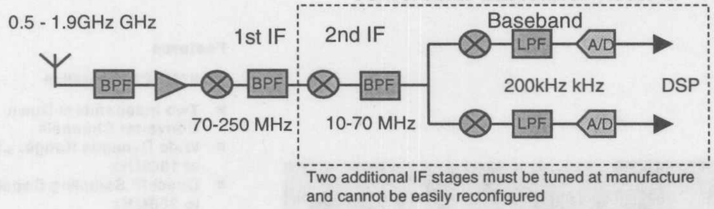
Parameter	ADC14061	ADC14161	ADC16061
SNR	**80dB**	**80dB**	**80dB**
S/N+D	**79dB**	**79dB**	**80B**
THD	**-88dB**	**-88dB**	**-88dB**
Power Consumption (typ/max)	**390/475mW**	**390/475mW**	**390/475mW**
INL (typ)	**± 2.5LSB**	**±2.5 LSB**	**±0.75 LSB**
DNL (typ)	**±0.35 LSB**	**±0.35 LSB**	**±0.35 LSB**
Offset Error	**16LSB**	**16LSB**	**16LSB**
FS Gain Error	**65LSB**	**65LSB**	**65LSB**

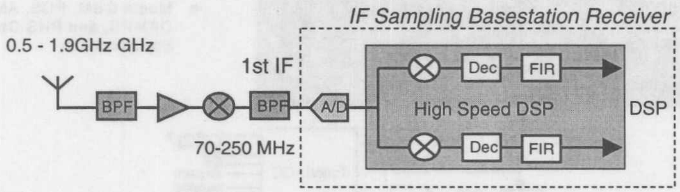
National Semiconductor *Analog Solutions* 33

These 14- and 16-bit, 2.5MSPS ADCs have excellent DNL and low offset and gain errors as their main features. These low errors can eliminate the need for manual adjustments in applications such as I/Q demodulation. Self-calibration allows for maintenance of accuracy over time and temperature.

High-Speed ADCs (and more) for IF Sampling

Conventional vs. IF Sampling Receivers





Direct IF sampling

- removes the need to tweak analog filters
- removes two mixer/filter/LO stages
- allows simple software reconfiguration
- provides near complete mixer image rejection

National Semiconductor   *Analog Solutions* 35

Conventional receivers use up to three stages of down conversion in the analog domain. Each stage requires a local oscillator (LO), a mixer, and a narrowband filter.

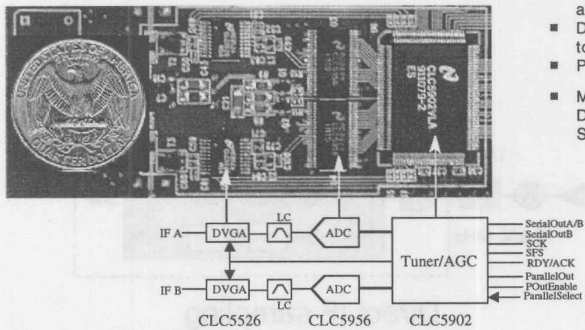
In a direct IF sampling receiver the ADC directly samples the result of the first mix down stage. SAW filters (requiring no tuning) typically follow the first mixer and the remainder of the tuning is performed digitally. These digital filters can be easily reprogrammed for different radio standards making this receiver very flexible.

Since the quadrature processing of the signals is done digitally there is no concern over component matching. Near perfect mixers are a benefit of this digital approach.

CLC5526, CLC5956, and CLC5902 Diversity Receiver Chipset

Features

- 52MSPS Operation
- Two Independent Down Converter Channels
- Wide Dynamic Range: >120dB at 150MHz
- Direct IF Sampling Capability to 300MHz
- Programmable AGC
- Meets GSM, PCS, AMPS, DAMPS, and PHS Cellular Specifications



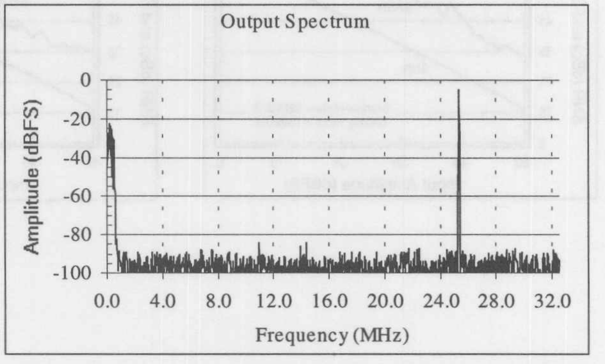
National Semiconductor   *Analog Solutions* 36

The Diversity Receiver Chipset (DRCS) enables direct sampling and downconversion of IF signals. The CLC5902 provides the digital equivalent of a local oscillator, mixer, and narrow bandwidth channel filter. The LO and channel filter are fully programmable allowing simple receiver design and manufacture. Multiple CLC5902s can be driven from a single ADC to facilitate wideband receiver designs. Use of LVDS components is a good way to distribute the ADC signals.

The digital AGC circuit in the CLC5902 provides a power detection circuit followed by programmable threshold and response-time circuitry. When the ADC output level crosses the programmable threshold the DVGA will reduce the input signal by 6dB. At the same time the circuitry in the CLC5902 will increase the gain by 6dB providing a linear output signal. The total dynamic range is the sum of the ADC SNR, the DVGA gain range, and the processing gain. There is a small reduction in dynamic range due to noise contributed by the DVGA. For GSM systems (52MSPS, 200kHz channel bandwidth) the full-scale to noise floor range is greater than 120dB.

CLC5956
12-bit, 65MSPS Broadband ADC

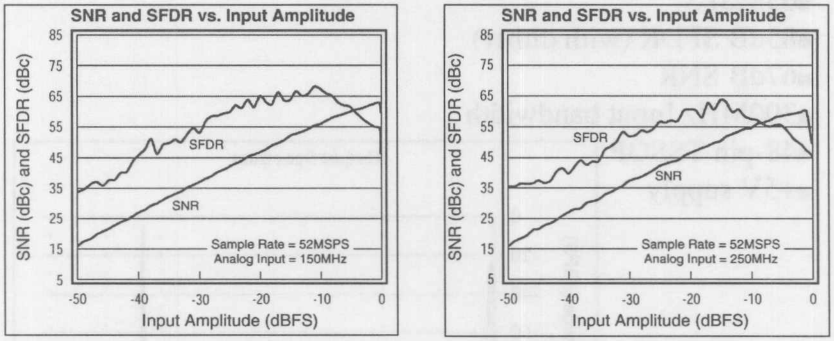
- 65MSPS
- 85dB SFDR (with dither)
- 67dB SNR
- 300MHz Input bandwidth
- 48-pin TSSOP
- +5V supply



The CLC5956 uses a pipelined architecture with multiple sub-ranging elements. With its 65MSPS sampling rate, 300MHz input bandwidth, and superior dynamic characteristics, it is ideal for such demanding applications as cellular basestations, digital communications, imaging, high-definition video, and electro-optics.

In order to support 65MSPS operation the capacitors in the sample and hold amplifiers must be very small, which limits the minimum usable sampling frequency to about 15MHz.

CLC5956 Operation at IF



National Semiconductor

Analog Solutions 38

Certain applications require more SNR while others require more SFDR. Try to operate the ADC with the highest input signal possible to improve SNR. As the plots illustrate SFDR can be improved by reducing the input amplitude slightly. Making the correct trade-off here can have a significant impact on system performance.

dBc - dB below carrier (or fundamental) level.

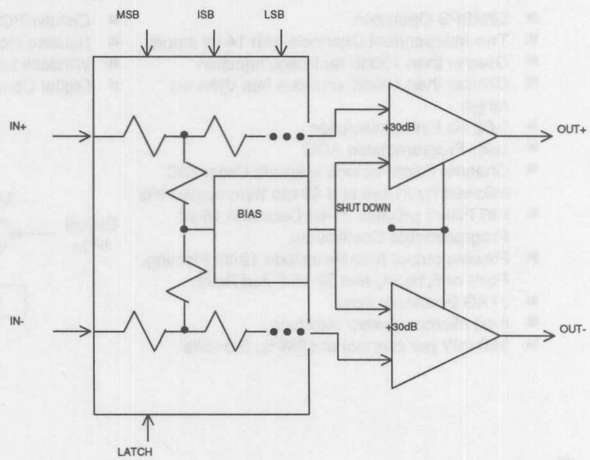
dBFS - dB below the ADC Full-Scale level.

SFDR - Spurious Free Dynamic Range. Includes all distortion terms. Typically in dBc.

SNR - Signal to Noise Ratio. Excludes harmonics. Typically in dBc. Add back the number of dB below full scale to get the noise floor or SNR in dBFS.

CLC5526
Digital Variable Gain Amplifier (DVGA)

- 350MHz Bandwidth
- Differential Input and Output
- LowTwo-Tone IM Distortion: -60dBc @ 1Vpp, 150MHz
- Low Noise: 2.5nV/ √Hz (max gain)
- Wide Gain Range: +30dB to -12dB
- Gain Control: Parallel w / data latching
- Gain Step Size: 6.02dB
- Supply Voltage +5V
- Supply Current 48mA
- 20 pin SSOP



The CLC5525 is a digital variable gain amplifier with excellent performance in a variety of high speed applications such as cellular basestations, medical imaging, IF sampling, back-channel modems, and high-definition video. It has differential inputs and outputs and is intended to be used with ac coupling at the inputs and outputs. It has a gain range from -12dB to +30dB in 6.02dB steps.

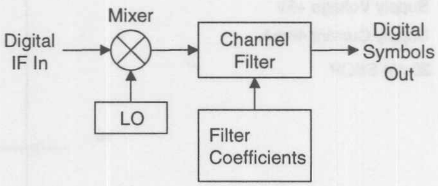
CLC5902
Digital Down Converter with AGC

Features

- 52MSPS Operation
- Two Independent Channels with 14-bit inputs
- Greater than 100dB far image rejection
- Greater than 100dB spurious free dynamic range
- 0.02 Hz tuning resolution
- User Programmable AGC
- Channel Filters include a Fourth Order CIC followed by 21-tap and 63-tap Symmetric FIRs
- FIR Filters process 21-bit Data with 16-bit Programmable Coefficients.
- Flexible output formats include 12-bit Floating Point or 8,16,24, and 32-bit Fixed Point.
- JTAG Boundary Scan
- 8-bit Microprocessor Interface
- 350 mW per channel at 52MHz, 3.3 volts

Applications

- Cellular/PCS
- Satellite Receivers
- Wireless Local Loop Receivers
- Digital Communications



National Semiconductor

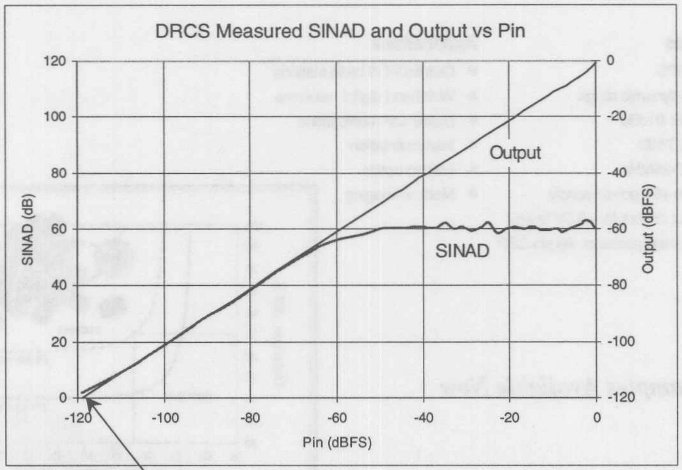
Analog Solutions 40

The Diversity Receiver Chipset provides the following features and benefits:

Feature	Benefit	Comments
1st IF Input Sampling	Eliminates 2nd IF downconverter hardware	1st IF frequency of ≥150MHz is desirable
Dual Diversity	Spatial diversity combats multipath and fading	Two antennas and maximal ratio combining provide 3dB SNR improvement
High Oversampling Ratio	Noise Processing gain in a narrowband channel Widely separated alias images	At f_s = 52Msps, the processing gain is 23dB and the 1st image is 26MHz away
Meet GSM spec's with optimized SAW configuration	Reduces SAW requirements	High dynamic range A/D can handle residual blocking signals remaining after filters
Discrete time channel filter in hardwired DSP	Eliminates narrow BW SAW filters	Narrow bandwidth channel filter realized in DDC
Wide dynamic range (>100dB) with "transparent" automatic gain control	Gain scaling of the input level is accomplished independent of the BTS receiver firmware	AGC parameters are fully programmable

DRCS Measured SINAD and Output vs. Pin

Combined ADC, DVGA, and Tuner/AGC Provide Extreme Dynamic Range



SINAD > 0 at -120dBFS (52MSPS, 200KHz Output BW)

This plot illustrates the linear output range provided by the DRCS.

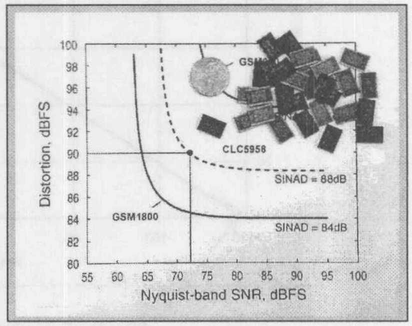
As the input signal approaches -60dBFS the DVGA will decrease the signal by 6dB. At the same time, the circuitry in the CLC5902 will increase the gain by 6dB providing a linear output signal. Since the ADC's SINAD is about 65dB for a 150MHz input the SINAD flattens out at this point. The DVGA gain range adds 42dB to the dynamic range but cannot increase the instantaneous SINAD. The DVGA merely moves the 65dB of instantaneous SINAD up and down the output signal line after the input exceeds -60dBFS.

CLC5958
14-bit, 52MSPS Monolithic A/D Converter

Features
- 52MSPS
- Wide dynamic range
  SFDR: 91dBc
  SNR: 71dB
- fin = 0-25MHz
- Single +5V power supply
- Output drivers for +3.3V to +5V
- Very small package: 48-pin CSP

Applications
- Cellular/PCS base stations
- Wideband digital receivers
- Digital communications
- Instrumentation
- Electro-optics
- Medical imaging

Samples Available Now



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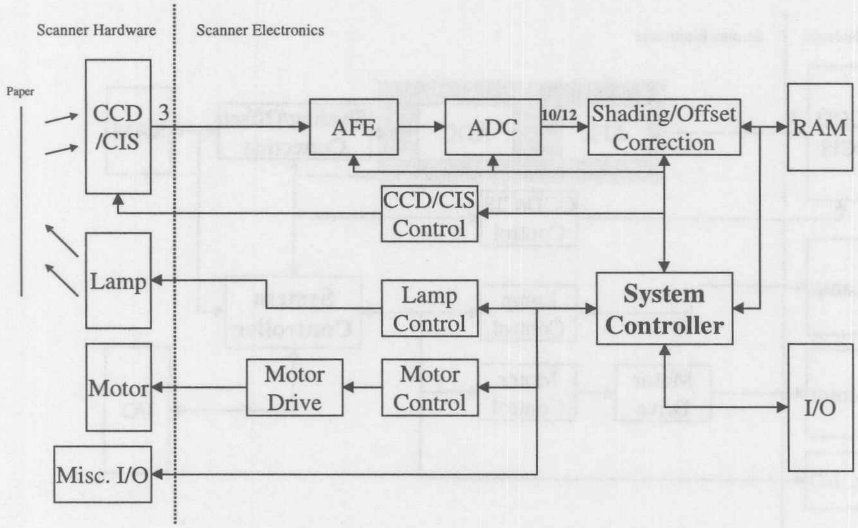
High-speed ADCs have opened up the possibility of wideband and software controlled multi-standard radio receivers. In a typical narrowband receiver the ADC digitizes only one carrier. In a wideband system the ADC digitizes a large portion of spectrum with multiple carriers. This requires much more dynamic range (SINAD) than a narrowband digitizer. Once the wideband signal is digitized a digital downconverter can be utilized to tune and filter each channel. In this scenario multiple downconverters can be connected to a single ADC greatly reducing the hardware required for a multi-channel receiver.

The plot above illustrates the requirements for an ADC to be used in a wideband GSM receiver. The CLC5958 provides sufficient SNR and Distortion performance to meet the GSM-1800 specification. Note that the channel filters reduce the noise from the Nyquist band SNR by about 20dB (processing gain from reducing the bandwidth by a factor of 192).

Typical Color Scanner System



This is a block diagram of all the electronics in a typical flatbed color scanner.

A linear CCD or CIS optical sensor transduces light into a voltage. This voltage, which represents light intensity, is present at the output of the sensor one pixel at a time.

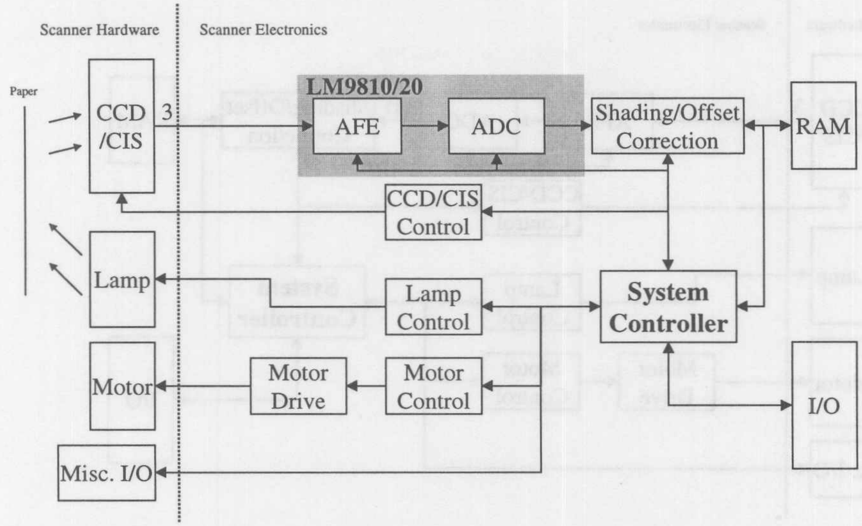
The sensor's output voltage is converted into pixel data by an analog-to-digital converter. An analog-front-end, or AFE, amplifies and adds or subtracts offset to the sensor's output signal to maximize the dynamic range of the ADC.

The converted pixel data must be corrected for sensor shading (gain) and offset errors. A pixel shading and offset coefficient is stored in RAM for each sensor element. Each ADC conversion result is linearly corrected by a digital addition and multiplication with correction coefficients that correspond to specific sensor elements.

A system controller must synchronize all the functions of the scanner and control data flow. The sensor control signals and the lamp on/off timing must be synchronized with the motor control as the sensor moves across the image. Conversion data, configuration data, and correction coefficients must be moved between RAM, I/O and all control blocks.

A PC controls the scanner and reads back image data through the scanner's I/O interface. The I/O interface is commonly Parallel Port, SCSI, and more recently, USB.

LM9810/20 Color Scanner System



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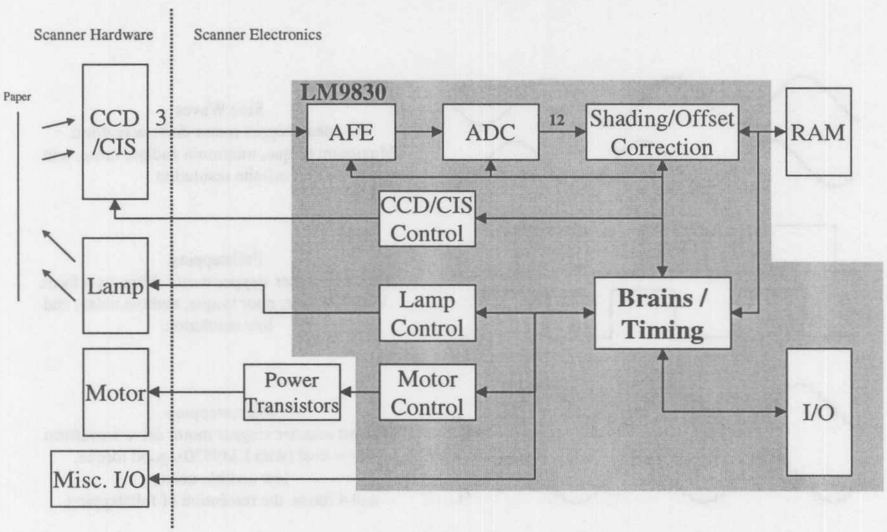
The LM9810 and the LM9820 perform all analog and mixed signal functions necessary to accurately digitize sensor output. These scanner analog front end's perform correlated double sampling, and have an integrated PGA, offset DAC, and an ADC. The LM9810 has a 6MHz, 10 bit ADC and the LM9820 has a 6MHz, 12 bit ADC.

The LM9810/20 allow experienced scanner designers to focus on the scanner's digital design. In a typical LM9810/20 scanner system, the shading/offset correction, and the CCD/CIS, lamp, motor, I/O, and system control are commonly integrated into one or two dense, digital ASICs.

LM9830 Color Scanner System



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The LM9830 is a complete scanner on a chip. The LM9830 (known as "Merlin" inside National Semiconductor) integrates all the analog, mixed signal and digital electronics (except for the RAM and the power transistors) necessary for a complete scanner.

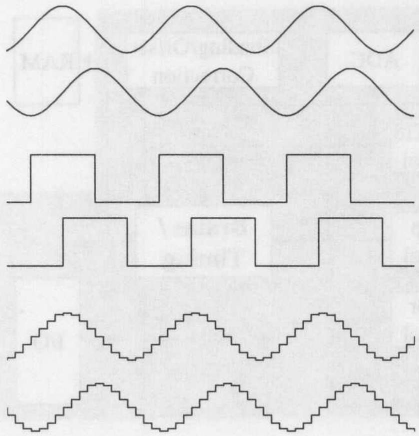
The design of the LM9830 had several goals. One was to produce a complete scanner chip that would enable smaller manufacturers to compete with the larger manufacturers in terms of component cost. A lot of smaller scanner companies don't have the R&D resources necessary to compete with the big guys. A single chip solution allows them to focus their resources on the mechanical and optical systems. To reduce their software burden, we also supply a working TWAIN driver (similar to the printer driver required for a printer) and source code. Customers can modify the TWAIN code as much as they want to add features, enhance performance, and otherwise differentiate themselves from their competition.

The other goal was to produce the highest-performing scanner electronics in its class ($300 and below). In this case, low cost and high performance were not mutually exclusive goals. By integrating the entire scanner onto one piece of silicon, we were able to provide significant features and performance enhancements that both substantially reduced the amount of time it takes to acquire an image and improved the quality of the final image.

The first area of improvement was in the stepper motor - the more precisely you can position the sensor with the stepper motor, the higher the vertical resolution the system is capable of. And the faster you can move the image sensor, the faster your scan. A technique known as microstepping allowed us to provide both, at negligible additional cost.

We also refined the image processing block and created a novel (and patent-pending) approach to matching the scan rate to the PC's I/O speed- but we'll save that for last. First let's look at microstepping.

Microstepping



Sine Waves
The ideal stepper motor drive waveform.
Maximum torque, minimum audible noise, and infinite resolution.

Fullstepping
Typical scanner stepper motor drive waveform.
Very low cost, poor torque, audible noise, and low resolution.

Microstepping
The best scanner stepper motor drive waveform.
Low cost (with LM9830), good torque, low audible noise,
and 4 times the resolution of fullstepping.

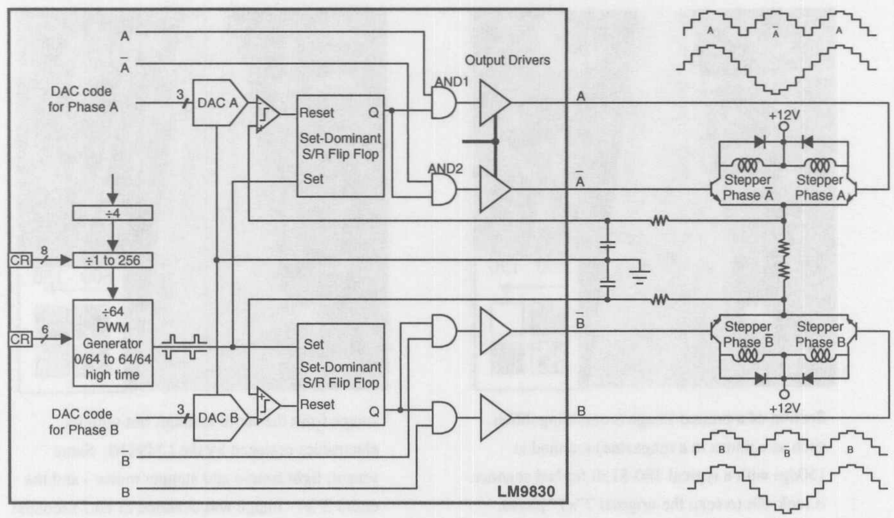
The stepper motor used to move the one dimensional image sensor across the image to create the second dimension requires a 2 phase high power control signal. When phase A leads phase B by 90°, the motor rotates in one direction and the sensor moves forward. When phase A lags phase B by 90°, the motor rotates in the opposite direction and the sensor moves in reverse.

The ideal waveform for these control signals are sine waves. Sine waves create constant movement with maximum torque, and their low harmonic content reduces the audible noise generated by the motor movement. Since there are an infinite number of angles between 0 and 360 degrees, the motor position can be determined with nearly infinite precision,. Since motor position determines vertical position in a scan, this maximizes the vertical resolution of the scanner.

In the extremely cost-conscious scanner market, a technique called "fullstepping" has been used in most low-end scanners. This substitutes a digital on/off for the sine waves. This works, but it limits the vertical resolution of the scanner to by allowing only 4 different positions/360 degrees. The non-sinusoidal drive signal reduces the torque generated by the motor, reducing the maximum possible scan speed, and increases the audible nosie, both due to the high harmonic content of the signal and the "jerkiness" of the motor movement. Its popularity in scanners is due to the fact that it is an extremely low cost solution, requiring only 4 power transistors driven by a digital logic-level signal.

Mid-range and higher-end scanners usually use a technique known as "microstepping". Microstepping approximates a sinewave by sensing and controlling the current in the motor winding. Microstepping motor controller ICs have been available for some time, but their cost is usually high, since they must combine power switches and digital control circuitry with a large amount of analog (digital-to-analog converters and comparators). This relatively high cost ($2-$5) has kept them out of the lowest range of scanners (street price of $80).

Microstepping



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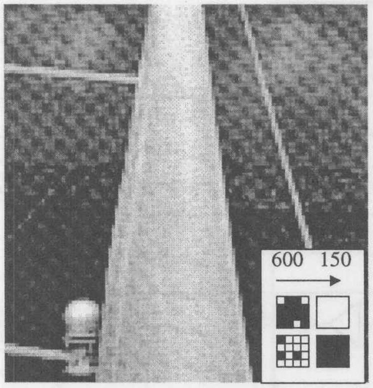
The mixed-signal nature of the LM9830 allowed us to integrate a microstepping controller for the cost of a full-step controller. All that was required was 2 additional 2 bit DACs, 2 comparators, and a bit of digital logic. The final microstepping solution used the same external 2003 power transistor array as the full stepping solution, so the external component cost remains about the same. The additional analog and digital circuitry needed for microstepping comprises a small portion of the LM9830's total die area. Thanks to system integration, a valuable (and previously expensive) performance enhancement is obtained for free!

Here's how it works. If A is high, and the SR flip-flop's Q output is high, then Q1 will turn on and force current through the A winding. The set-dominant SR flip-flop is set periodically by a programmable pulse stream. If the A input is high, this will turn on Q1, which will then stay on until the flip-flop is reset. When Q1 is on, the current through the inductor rises. This current is sensed through R1, and low-pass filtered by R2 and C1. When the voltage across R1 reaches the DAC voltage, Comparator A changes states and resets the flip-flop.

If the DAC voltage is swept at a constant rate through 0, 0.191, 0.353, 0.462, 0.5, 0.462, 0.353, 0.191, and 0V, it will force a current through the motor winding that looks like the positive half of a sine wave. To create the negative half of the sine wave, winding A is switched off and the same current is forced the A*, which is the same as winding A but wound to create the opposite polarity magnetic field.

The same operations are happening for phase B, only 90° out of phase.

Image Quality
(It's What Meets the Eye)



Section of a printed image (containing dither, such as a photo in a magazine) scanned at 150dpi with a typical $80-$150 flatbed scanner. It took 40s to scan the original 3"x7" photo.

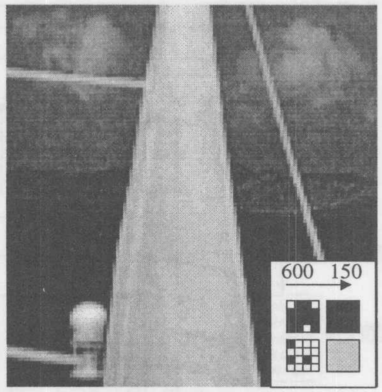


Image from the same scanner, but with its electronics replaced by the LM9830. Same sensor, light source and stepper motor - and the entire 3"x7" image was scanned in 10.7 seconds!

Another advantage of integrating an entire scanner system onto one IC was the freedom it gave us to process the signal. The LM9830 provides high quality images at all resolutions - not just the optical resolution of the scanner.

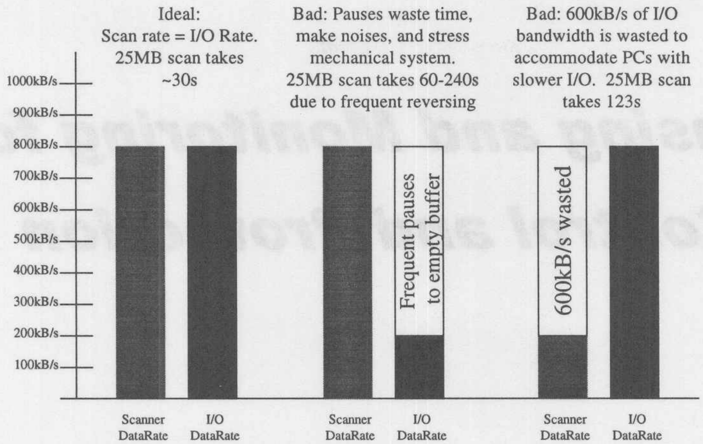
Most scanners scan images at only one resolution, the optical resolution (usually 300 or 600 dpi). To get to other resolutions (200, 150, 100, 75, etc.), they throw away pixels. If you're scanning at 600dpi, but you discard 3 out of every 4 pixels (and 3 out every 4 entire lines), the resulting image will be at 150dpi.

But to get to 150dpi, you've thrown away 15 out of 16 600dpi pixels - that's 94% of the original image! This can create aliasing problems. What if the 4x4 array of 600dpi pixels was mostly black, but the pixel in the upper left corner (the pixel kept for the 150dpi image) was white? After the other 15 pixels were discarded, the pixel remaining would be white, despite the fact that the majority of pixels inside that 150dpi area were black. This is demonstrated in the image on the left.

National's LM9830 doesn't throw away pixels to reduce resolution - it averages them, the same way the human eye averages distant images. So if the 4x4 600dpi pixel array is mostly black, the resulting 150dpi pixel will also be mostly black (dark gray). If the original is mostly white, the 150dpi pixel will be light gray.

Having total control over both the analog and digital design of the system allowed National to optimize image quality for any set of scan parameters - and without compromising scan speed, as you'll see next.

Printer Port I/O Limitations



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The fastest scan speed theoretically possible for a given PC is easily determined by the dividing the image size by the PC's I/O data rate. A 300dpi color scan of a letter-sized page is about 24megabytes (300x8.5"x300x11"x3bytes/pixel = 24.08MB). If the PC's data rate is 800kB/s, then the image must take a minimum of 24MB/800kB = 30.8s to scan and transfer to the PC.

Scanners have traditionally scanned at a fixed data rate. This makes the scanner easier to design and manufacture, but the problem is that the speed of a given scan is rarely close to the speed of the PC's I/O. Parallel port I/O speeds range from less than 50kB/s (nibble mode), to almost 1000kB/s (EPP or ECP mode). A scanner must support this range of speeds to be compatible with the installed base, old and new, of PCs.

But what should a scanner designer fix the data rate at? If it's too fast, the scanner must pause to prevent an overflow of its internal buffer. Recovering from a pause usually means reversing, then resuming forward motion to remove gear lash and prevent distortion of the image. Pauses waste time, make additional undesirable noises, and significantly increase the wear on the mechanical system. For that reason scanner designers try to minimize pauses.

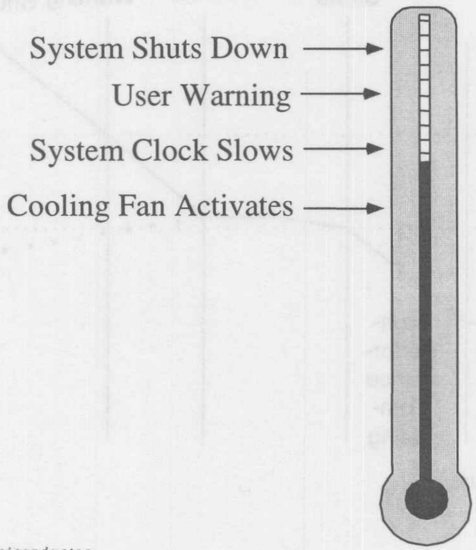
Unfortunately, the way pauses are often eliminated is by slowing down the scan speed to a compromise that will give barely tolerable scan times for PCs with fast I/O rates (in the example above, the scan time would be 24MB/200kB/s = 123s - 4 times longer than the theoretical!), and a barely tolerable amount of reversing for PCs with slower I/O. The result is that the only time you get optimum scan speed is when by chance your I/O rate happens to be the same as the scanner's rate.

The LM9830's philosophy is to measure the PC's I/O rate and adjust the scan speed so it generates data at a slightly lower rate. This optimizes the scan time so that the user will always get a scan time close to the ideal, regardless of the PC's I/O rate. The LM9830's revolutionary combination of analog and digital hardware enables this to happen.

Sensing and Monitoring for Control and Protection

National Semiconductor

Thermal Management in Electronic Systems



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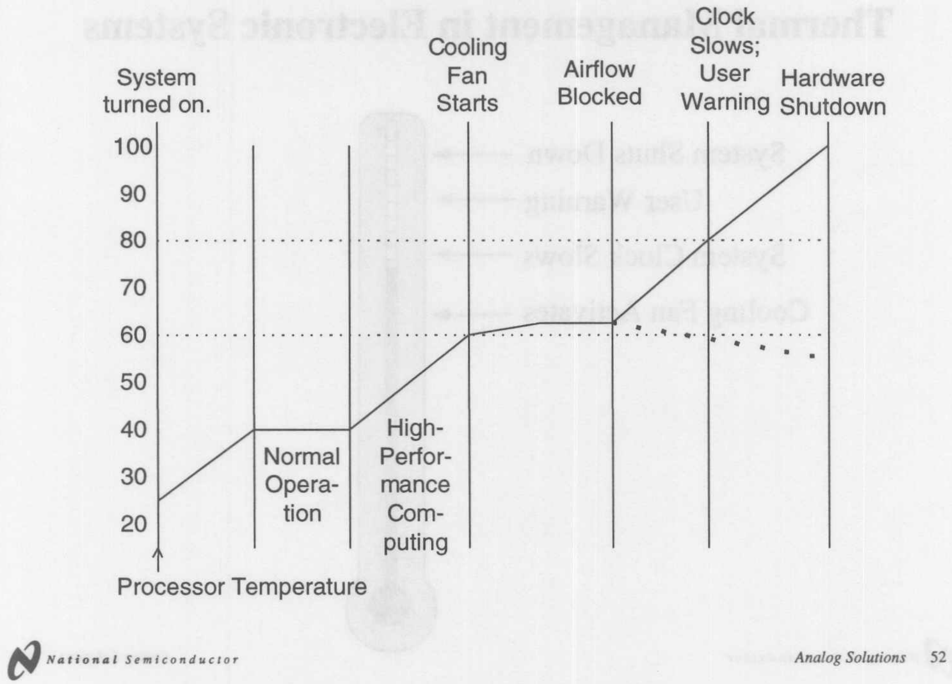
Managing heat in a complex system requires appropriate hardware and software. If the potential for excessive temperature exists, an appropriate sensor should be used to monitor the temperature of critical components.

As temperature increases, various techniques may be used to reduce it. For example, some systems may not use a cooling fan during normal operation (to minimize acoustical noise), but a fan may be activated if temperature exceeds a specified point.If temperature continues to climb, another thermal control method, such as slowing the system clock, may be invoked. This will reduce system performance, but will also reduce temperature.

Note that these techniques will not be appropriate in every system. Some systems may not be able to tolerate fan noise even in a "near meltdown" situation. Others may not be able to tolerate a reduction in processing power caused by slowing the clock.

At some point, the temperature may be high enough that the system needs to begin a "graceful shutdown", possibly saving data or warning the user of the high-temperature conditions.

All of the actions described so far would typically be under software control. If a serious fault condition persists and control software is no longer operating properly, the final safety measure will be to shut the system down directly by turning off power supplies with a hard-wired logic output from the temperature sensor. This bypasses software completely and is very reliable.

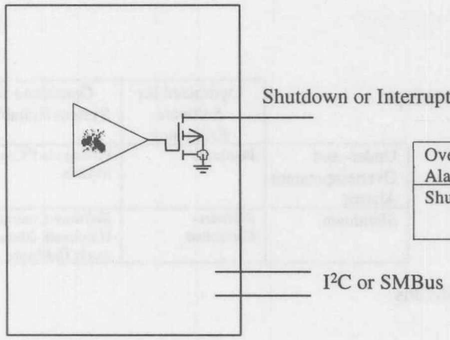


Here's an example of a system in operation. This example might apply to a PC, a lab instrument, or some other type of electronic system. After startup, operating under nominal conditions, the system may need no cooling of any kind. At some point, heavier demands may be placed on the system that cause its temperature to rise significantly. When the temperature is high enough, a cooling fan may be necessary to actively cool the system. This will reduce temperature by several degrees and is often sufficient to ensure safe long-term operation.

If something unusual happens that prevents the fan from operating properly, such as fan failure or airflow blockage, the fan will be unable to keep the system's temperature within the safe range. At this point, power dissipation may be reduced to minimize heating. In a system whose primary heat source is a microprocessor, power dissipation can be easily reduced by slowing the processor clock. If this doesn't reduce temperature sufficiently, the system may need to be shut down until the cause of the problem can be identified and fixed.

This approach is similar to the recommendations included in the ACPI specification for PCs, although ACPI makes certain assumptions that do not apply to all systems. For example, ACPI assumes that the operating system and thermal control software are always functioning properly. This is not necessarily the case, which is why we also recommend a hard-wired system shutdown controlled by the temperature sensor.

Single-Comparator Sensors



	Optimized for Software Efficiency	Optimized for System Reliability
Overtemperature Alarms	Interrupts	Polling via I²C or SMBus
Shutdown	Software-Controlled	Software-Controlled If software doesn't work: Hardware

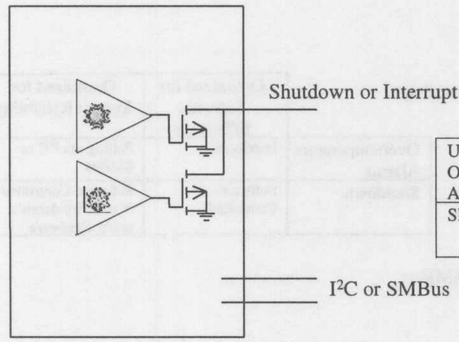
Digital temperature sensors are available with a variety of output configurations that are useful in system protection applications. Simpler devices like the LM75, have a single open-drain output that can be used as an interrupt, an alarm driver, or a shutdown signal. How you use this pin depends on the nature of the system and the relative importance of fail-safe thermal protection versus software efficiency.

If you want a system that spends very little time communicating with the temperature sensor, you can set the LM75's internal digital comparator to trigger an interrupt only when the temperature rises above a value that demands attention from the system's processor. Therefore, under normal operating conditions, the system will never have to communicate with the temperature sensor (except at startup, when the comparator threshold will be set). However, if the processor ever stops working properly (or the software has a problem), the system may never know that there is a thermal problem and may therefore never act to reduce power dissipation.

Alternatively, you could set up your system so that the processor polls the temperature sensor periodically to detect incipient thermal problems. The comparator output can then be connected to the system power supply and completely shut down the system if temperature gets excessively high. This type of system will always shut down in the event of thermal problems, even in the presence of processor and software failures.

Two Comparators, One Output

Similar, but you can also have low-temperature alarms.

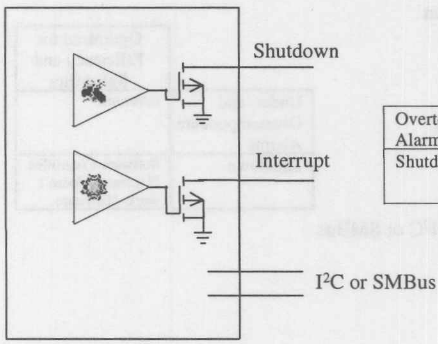


	Optimized for Software Efficiency	Optimized for System Reliability
Under- and Overtemperature Alarms	Interrupts	Polling via I^2C or SMBus
Shutdown	Software-Controlled	Software-Controlled If software doesn't work: Hardware

Some digital temperature sensors provide a single comparator/inerrupt output that is driven by two comparators, one set to an upper threshold, and one to a lower threshold. Such a scheme can be helpful in interrupt-driven systems where it is useful to know that the temperature has dropped below a “cold” threshold.

Two Comparators, Two Outputs

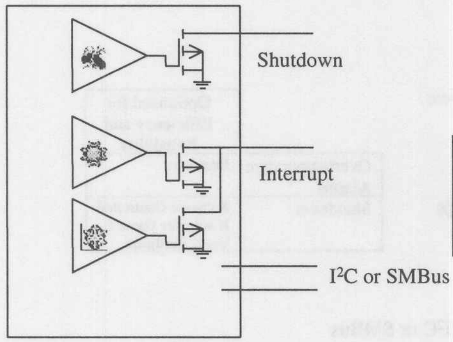
Efficient and Reliable



	Optimized for Efficiency and Reliability
Overtemperature Alarms	Interrupts
Shutdown	Software-Controlled If software doesn't work: Hardware

A sensor with two overtemperature outputs can help with software efficiency and with reliability. One output can notify the system's microprocessor of thermal problems, allowing it to change operating characteristics in an attempt to reduce temperature. The other output can be hard-wired to a power supply shutdown pin so that if thermal control efforts prove futile or if the system is not functioning properly, it will shut down before damage occurs.

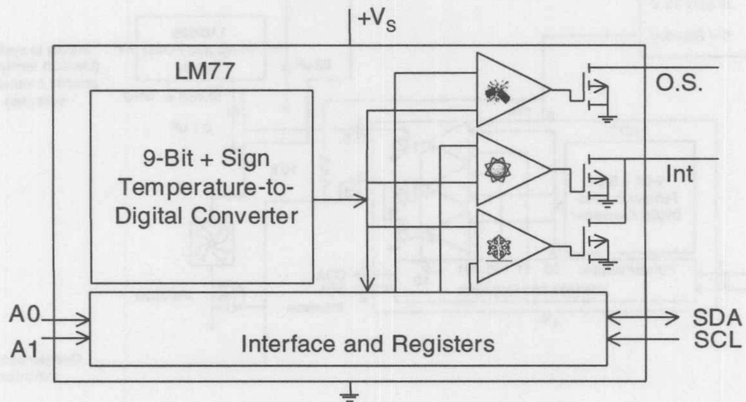
Three Comparators, Two Outputs



	Optimized for Efficiency and Reliability
Under- and Overtemperature Alarms	Interrupts
Shutdown	Software-Controlled If software doesn't work: Hardware

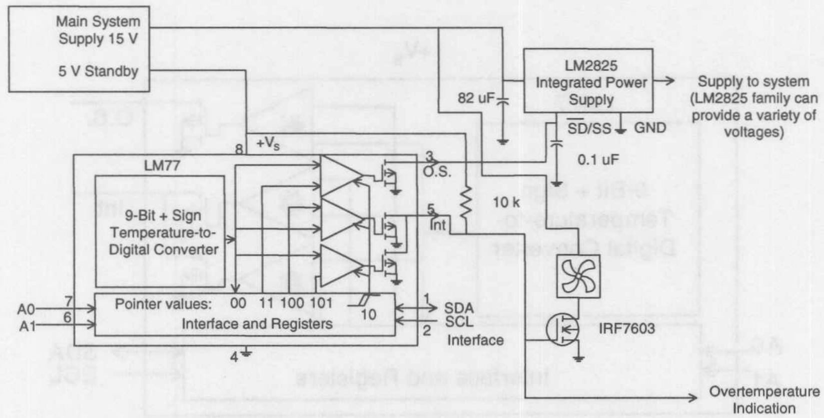
An even better approach adds a "cold threshold" sensor to the previous scheme, allowing the processor to be alerted of positive and negative changes in temperature.

Digital Temperature Sensor Optimized for System Reliability



This is an example of a temperature sensor that works as described on the previous page. Note the two "comparator" outputs. One can alert the system of out-of-range conditions and the other can be hard-wired to shut the system down in the event of dangerous high-temperature conditions.

LM77 Provides Thermal Warning, Control, and Protection



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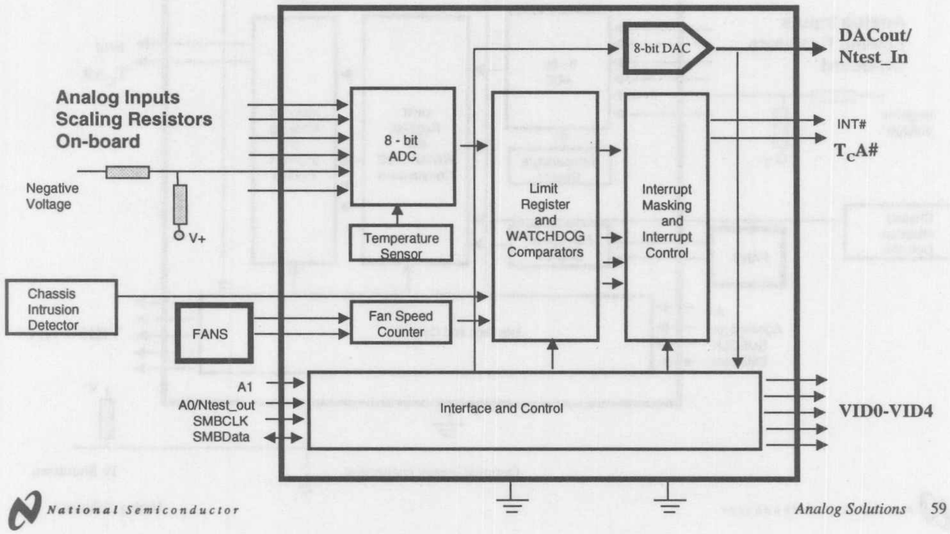
The LM77 can help realize the functions of Thermal Warning, Control, and Protection in Systems besides PC's. This example uses an LM77 to control a fan, an function that dictates the LM77 be operated in its default Comparator mode, and setting the LM77 window comparator low limit to a very low temperature. The high limit would be all that is required for controlling the fan. The output of the LM77 can be fed to the controller so that the controller is aware of what is going on. Keep in mind that since the LM77 is not in Interrupt mode the controller cannot reset this line.

The simple connection with a logic-level MOSFET at the INT output of the LM77 also requires properly setting the INT output Polarity in the Configuration Register of the LM77. Prior to setting the polarity to its inverted condition, the default state is active-low, an acceptable state since the default will be with fan power on.

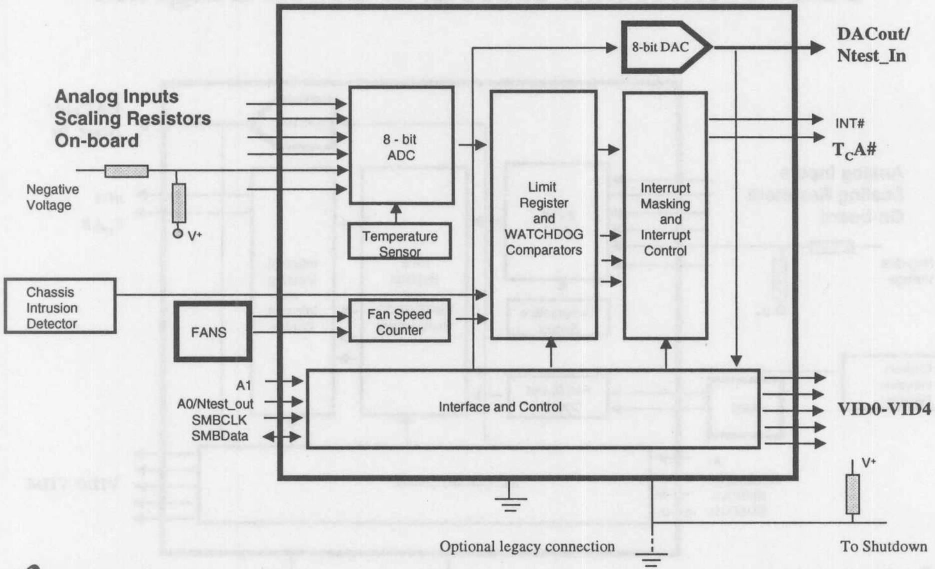
For further protection the O.S. output of the LM77 is fed to the Shutdown input of a Simple Switcher Integrated Power Supply. The LM77 should be continously fed by a standby power supply. This arrangement will turn the portion of the system responsible for the overheating off in the event that thermal control measures have failed.

Temperature Sensing, Voltage Monitoring, and Fan Monitoring: Heceta II Block Diagram



This Heceta II-compliant system monitor chip was designed primarily for PC applications, but is useful in a variety of systems. It has all of the normal system monitor functions (analog inputs for power supply monitoring, fan speed counters, a DAC output for controlling fan speed) plus an interrupt for identifying increases in temperature without constant polling and an additional output that can be used for hardware shutdown. Unfortunately, it has no shutdown output, so its interrupt output must be used for shutdown.

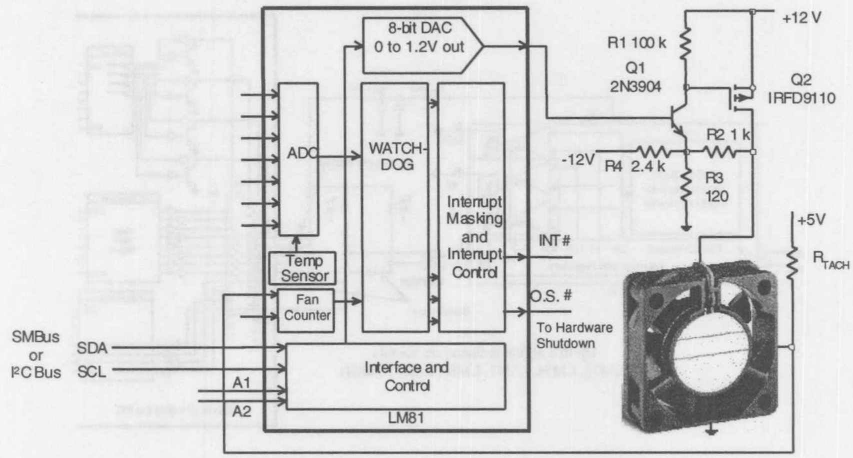
LM81: Three Comparators, Two Outputs



The LM81 provides a TCA, or TCritical Alert, output that is not available on other Heceta II implementations. The TCA output is on a pin that must go to ground for the other Heceta II devices. TCA allows the LM81 to operate as a three-comparator, two-output temperature sensor (in addition to all of its other functions). This makes it much more convenient to use in systems that need foolproof overtemperature shutdown capability.

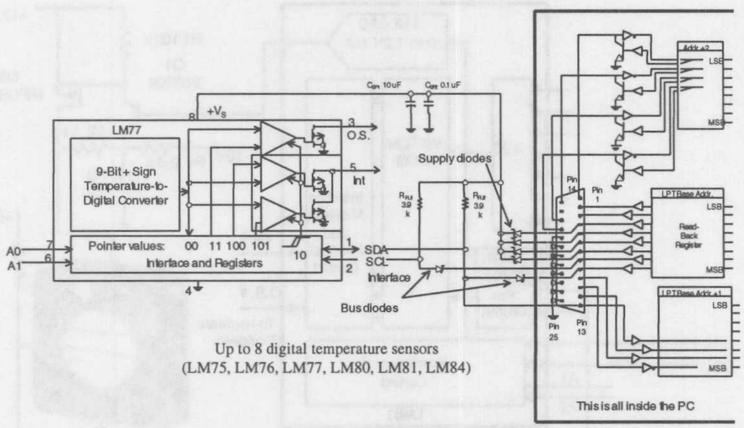
This depicts how a board might be designed to accept either the LM81 or earlier Heceta II implementations.

Fan Control With the LM81's DAC



The DAC output of the LM81 can be used to control the speed of a cooling fan by adding a handful of low-cost external components. By controlling fan speed, active cooling can be done without generating excessive noise.

Multiple Sensors on the Parallel Printer Port



Up to 8 digital temperature sensors
(LM75, LM76, LM77, LM80, LM81, LM84)

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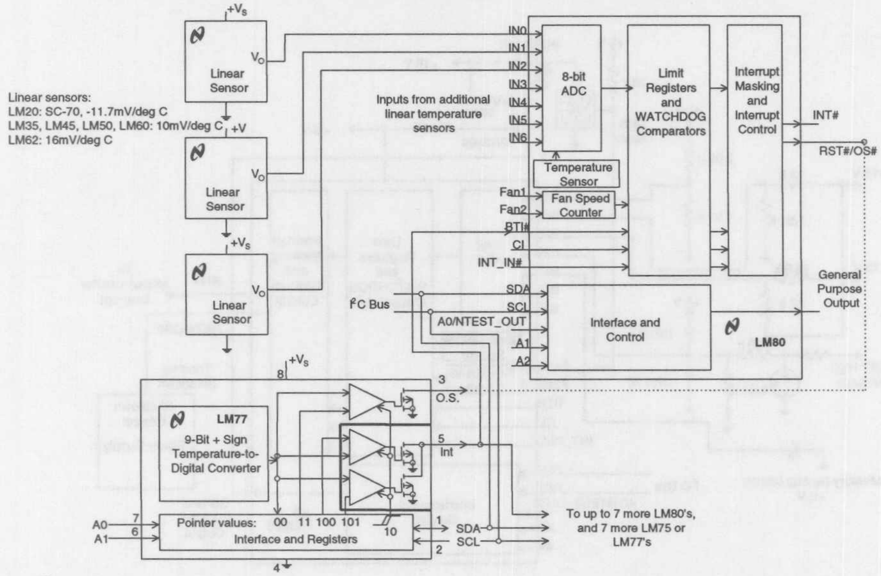
The Parallel Printer Port on the PC is a convenient way of getting data into and out of a PC. Using the Parallel Printer Port avoids the need to remove the lid on desktop computers to install interface cards, not to mention the fact that you can't do that anyway on laptops.

The Parallel Port is actually three ports. The latest computers have an 8-bit bi-directional port; a 4-bit output port (open collector, but often with strong pull-up); and a 4-bit input port. The section of the schematic labeled "This is all inside the PC" gives some idea of how each bit is mapped to it's specific register and how the registers are mapped to the I/O space of the computer.

We generate our I2C interface by using Schottky diodes to "mimic" an open-collector output. The data is read back into the input port. Because the power consumption of our devices is so low, they can readily be powered off the port, and in this case every spare line is diode summed into the power supply line for the LM77.

64 Temperatures via I^{2}C



National Semiconductor *Analog Solutions* 63

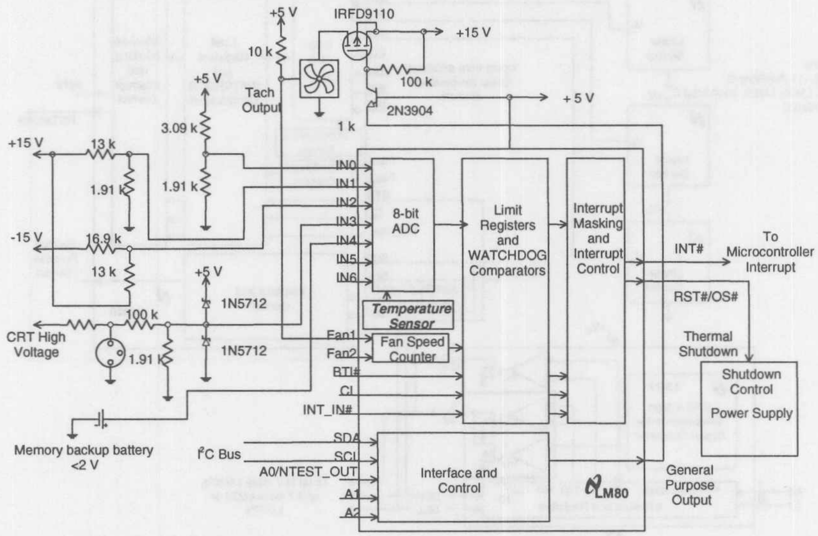
Our digital temperature sensors and hardware monitors are truly Data Acquisition Systems, a fact readily brought to light by this circuit which demonstrates how much data can be acquired through the simple two wire serial I^{2}C bus.

Besides the digital sensors on the bus, the LM80 can digitize the output of a variety of linear sensors. Linear sensors may be desirable because their packaging allows them to be located in positions where it might be difficult to install a digital sensor.

When using linear sensors the most straightforward connection is the 10 mV/°C sensors to match the 10 mV LSB of the LM80, resulting in a relationship of 1 LSB = 1°C. Other sensors are readily interfaced, but their different analog scaling will require some number crunching in software.

When connecting a large number of devices to the I^{2}C bus remember to either observe the maximum bus capacitance restriction of 400 pF, or buffer the bus (ICs are available from other vendors to do this).

LM80 Data Acquisition: Instrument Health Monitor



National Semiconductor *Analog Solutions* 64

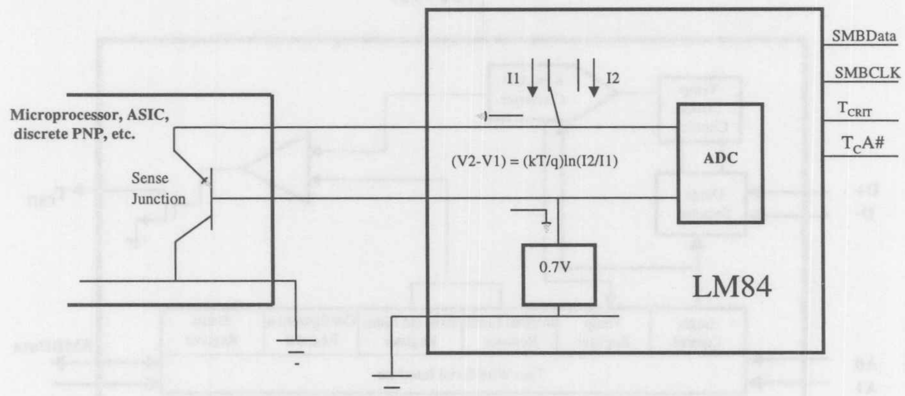
To further illustrate that Hardware, or Health Monitors are truly Data Acquisition Systems consider their use in instruments and test equipment. In this example an LM80 is used to monitor critical voltages in a system, temperature, and fan speed.

Among the voltages that could be monitored include all the various supply voltages, the supply of the LM80 itself, possibly the voltage of backup batteries.

When monitoring high voltages such as a CRT voltages, protection is necessary to avoid damage to the LM80. In the example shown, a neon lamp provides the first mechanism for protection, supported by Schottky clamping diodes to both supply rails.

The General Purpose Output of the LM80, a line which can be activated or de-activated by the system controller, is illustrated for use here in controlling a fan. A good example of this might be a high-power bench power supply. Often these supplies require noisy fans, and keeping them off when not needed is of great value to the end user. A fan controller compatible with a tachometer output requires a high-side drive at 12 or more volts. The cascode connection on the General Purpose Output is a simple way of coupling that output to the high side device while observing voltage restrictions on the LM80.

Sensing Temperature of an External PN Junction



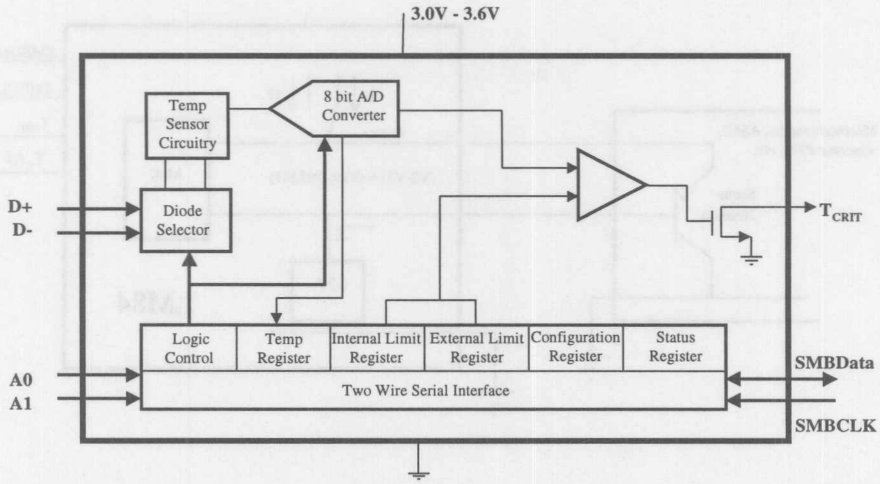
Some newer digital temperature sensors can sense the temperature of a PN junction external to the sensor chip. This capability was driven by the needs of the PC industry.

The CPU dissipates so much power and is so expensive that most of the thermal monitoring design effort focuses on sensing the CPU's temperature. While it is possible to estimate the die temperature of the CPU by mounting a temperature sensor near it, a more accurate approach is to sense CPU temperature directly using a PN junction on the CPU die itself. This is illustrated above.

The PNP transistor on the left resides on the CPU and is driven by the temperature sensor chip on the right. The sensor chip alternately sends two currents through the emitter-base junction of the sense diode. The current sources are usually designed to have an accurate ratio of about 10:1. By measuring the voltage across the junction at each current level, the temperature of the junction can be calculated. A temperature sensor chip that does this is often referred to as a "remote diode temperature sensor".

Note that a remote diode sensor can also detect the temperature of non-CPU devices. Many ASICs, especially those with power functions, for example, can be protected against thermal problems by a remote diode sensor.

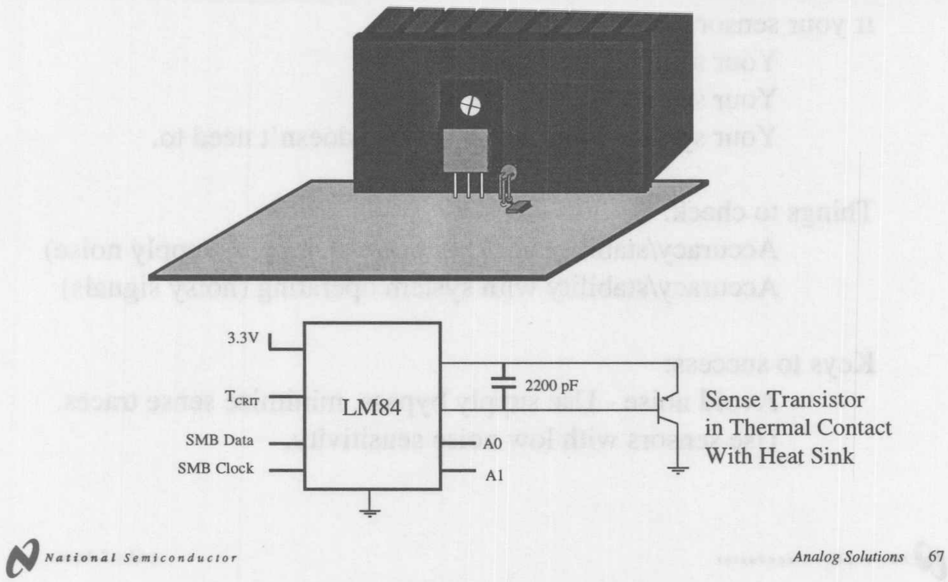
LM84 Block Diagram



The MAX1617 was the first remote-diode temperature sensor on the market. It includes an internal temperature sensor that measures the temperature of the IC itself so that the IC can report the temperature of the CPU and the PCB.

The LM84 is a new remote-diode sensor for low-cost systems. To keep costs low, the LM84 is missing three features compared to the MAX1617: the shutdown function, the low-temperature comparator (not necessary if you're using the Alert output to shut the system down), and the SMBus Alert Response function (again, not necessary when the Alert output shuts the system down).

Added, but invisible, features include a reliable sensing technology for excellent noise rejection and SMBus™ timeout to prevent bus lockup in the event of a communications error.



A remote diode temperature sensor can also be useful for monitoring the temperature of a heat sink, as shown here. A PNP is mounted in the appropriate location on the heat sink and the LM84 senses its temperature.

The LM84 was designed to be the lowest-cost and most reliable remote diode sensor. Its temperature sensing technique makes it far less susceptible to power supply and radiated noise than other remote diode sensors.

Accuracy Matters!

If your sensor is inaccurate:

- Your system is too noisy.
- Your system is too slow.
- Your system shuts down when it doesn't need to.

Things to check:

- Accuracy/stability with your power supply (supply noise)
- Accuracy/stability with system operating (noisy signals)

Keys to success:

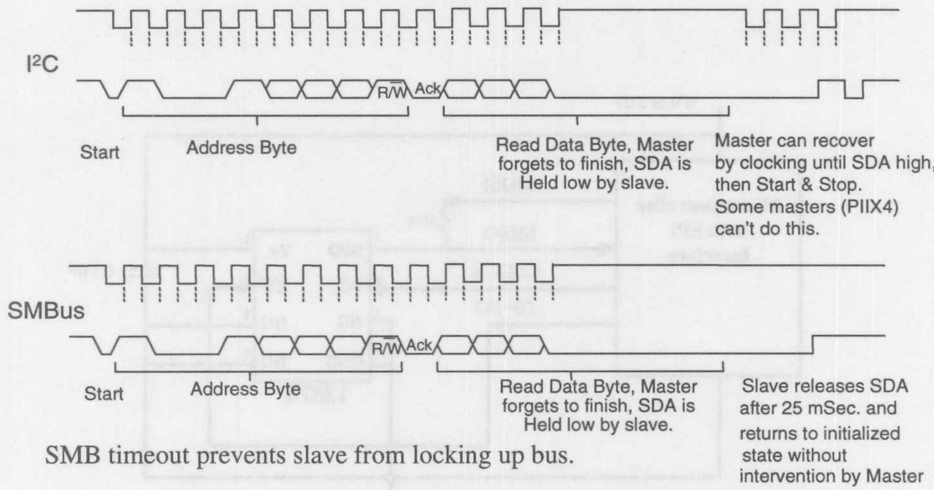
- Avoid noise - Use supply bypass, minimize sense traces.
- Use sensors with low noise sensitivity.

Accuracy in remote-diode sensors can be impaired by high sensitivity to noise, either on the power supply or on the diode sense lines. Why should you care? Because a sensor that gives unreliable readings due to poor sensor accuracy or poor noise rejection will force you to set your thermal shutdown trip points lower. This means the fan will turn on earlier, making your system noisier. The clock frequency will drop sooner, making your system slower. Your system will shut down when it is still capable of safely operating, or it might continue operating when the chassis is running too hot.

Always check the repeatability and accuracy of your sensor in a real system, not in a "clean" test box. Real system noise can degrade sensor accuracy in circuits that have poor noise rejection. National's digital temperature sensors use a delta-sigma ADC architecture with differential inputs that rejects supply and common-mode input noise.

Of course, you should try to minimize noise in your system by cleaning up the power supply for analog component like the temperature sensor. You should also use short PCB traces between a remote-diode sensor and the target sense junction.

I^2C vs SMB



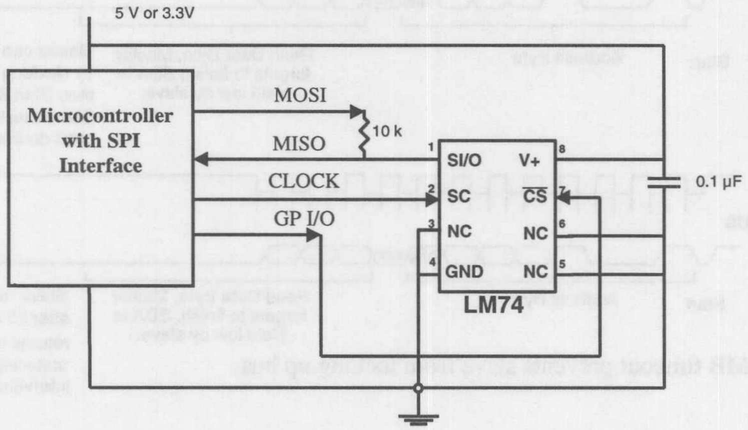
SMB timeout prevents slave from locking up bus.

I2C and SMBus are related, but different, standards. Besides using different logic levels, the two standards differ in their approach to communication errors. Some kinds of communications errors cause the slave (the temperature sensor IC) to hold the SDA line (the data I/O line) low, thus preventing any communications on the bus. For example, a missing clock pulse can cause this to happen. I^2C masters are expected to detect and correct such errors, usually by transmitting additional clock pulses until the error is cleared.

However, the masters used in many PCs are SMBus devices. The SMBus specification calls for the slave to correct any "stuck" bits by releasing the bus if it has been held low for an excessive period of time. When an I^2C sensor is used with an SMBus master, there is a possibility of a hung bus because there is no way to overcome a "stuck" I^2C slave.

The LM84 includes an SMBus timeout function that releases the SDA line after it has been held low for 25ms.

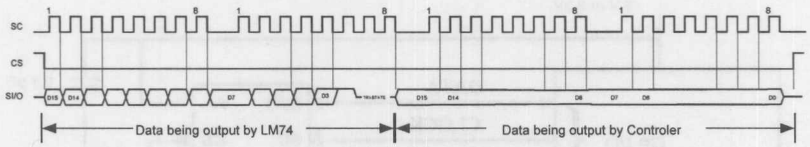
LM74 Read and Write Connection for SPI and MICROWIRE™



The LM74 is a very low-cost, accurate (12 bits, 1 degree C tolerance) digital temperature sensor with a Microwire or SPI™ interface for systems that do not have I2C readily available. It is shown here connected to an SPI microcontroller. Although the LM74 has a single I/O pin, it can interface correctly with an SPI microcontroller using this circuit.

Standard SPI™ and MICROWIRE™ interfaces have separate I/O pins for data input and output. If shutdown is required then the SI/O pin should be directly connected to the master input pin. A 10k resistor should be connected between the SI/O pin and the master output pin. During the first 16 clock periods of communication the LM74 will win the battle of communication. The master output should be in a high state during this time. During the second 16 clock periods the SI/O pin will be in high impedance state so the master will win the battle.

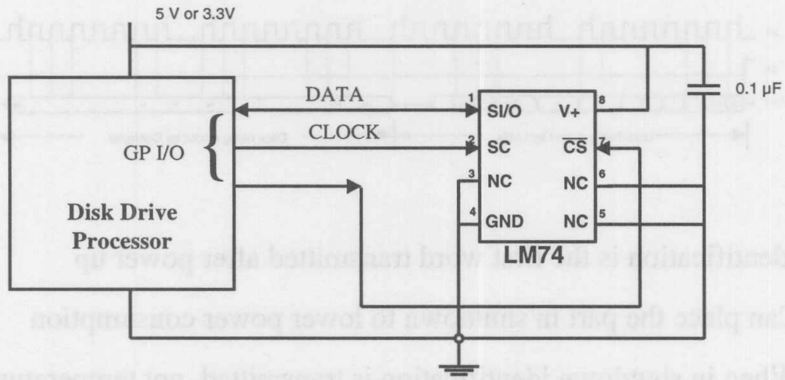
SPI/MICROWIRE Compatible Interface



- Identification is the first word transmitted after power up
- Can place the part in shutdown to lower power consumption
- When in shutdown identification is transmitted, not temperature data

The LM74 has a very simple interface. There are no user-programmable comparator registers or other functions that could add complexity. A typical I/O cycle will take a total of 32 clock periods. The LM74 shifts data out on the falling edge of serial clock (SC) and shifts in data on the rising edge of SC. After CS is brought low the LM74 will transmit data for the first 14 clock periods. For the next 10 clock periods the LM74 I/O line goes into a high impedance state. During the last 8 clock periods the LM74 listens to what is being transmitted. The LM74 has a bi-directional I/O pin.

The only command that the user has available is to place the device in shutdown in order to lower power consumption and read the identification register. If shutdown is unnecessary then writing to the LM74 will never be required and the SI/O pin can be used as an output only. When in shutdown, the LM74 will always transmit identification data. CS can be taken high at anytime during the communication sequence. A write to the LM74 is optional, the LM74 retains its shutdown/awake state until commanded to change. The LM74 requires that all 16 bits be clocked in before changing state. So if CS were bought high in the middle of a write sequence the LM74 would retain its state.



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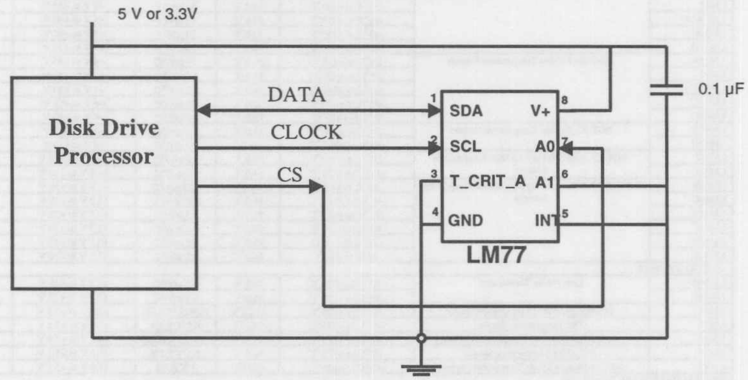
Disk drive reliability can be compromised at high operating temperatures. In many computer systems, failures in cooling components (such as clogged filters on fans, failed air conditioning) can go undetected for an extended time. The resulting stress can lead to unexpected failures and even data loss. Continuous operating temperature also directly affects the long-term failure rate. To prevent early failures from happening, high-temperature conditions can be reported to the host system using a temperature sensor such as the LM74. The host system can then be used to notify the user or system administrator to take action thus reducing the amount of time that may take place in detecting the failure.

LM77 in LM74 Socket



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The LM74 and the LM77 have compatible pin connections. Although one communicates via I²C and the other uses Microwire/SPI, the LM77 can serve as a drop-in replacement for the LM74 if software is configured as described below.

The figure above shows the LM77 as a drop in replacement for the LM74. Firmware can be used to determine which device is in place. The firmware should follow the following procedure:

1. Set the CS line high

2. Assume that a LM77 is in place.

3. Send out the I²C address of 1001001 with a read instruction of the LM77.

4. Receiving an acknowledge would confirm that the LM77 is in place. If an acknowledge is not received then the firmware should assume that an LM74 is in place.

Redundant confirmation that the LM74 is in place can be accomplished by reading the ID register of the LM74 by placing the LM74 in shutdown and then reading it's output. This would be the most robust implementation. The current samples of the LM74 will not output the ID when in shutdown. They output the last conversion data.

Temperature Sensor Selection Guide

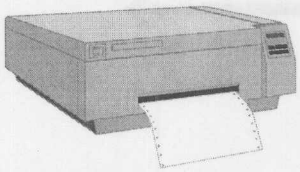
Product	Product Description	Operating Temp. Range	Accuracy	Sensor Gain	Supply Voltage Range	Quiescent Current
ANALOG OUTPUT						
LM20B	SC-70 Precision Celsius Temperature Sensors	-55 °C to +125 °F	±2.5 °C	-11 mV/°C	+2.4 V to +5.5 V	7 µA
LM20C		-55 °C to +125 °F	±5.0 °C	-11 mV/°C	+2.4 V to +5.5 V	7 µA
LM34A	Precision Farenheit Temperature Sensors	-50 °F to +300 °F	±2.0 °F	10 mV/°F	+5 V to +30 V	163 µA
LM34		-50 °F to +300 °F	±3.0 °F	10 mV/°F	+5 V to +30 V	181 µA
LM34CA		-40 °F to +230 °F	±3.0 °F	10 mV/°F	+5 V to +30 V	142 µA
LM34C		-40 °F to +230 °F	±3.0 °F	10 mV/°F	+5 V to +30 V	159 µA
LM34D		-32 °F to +212 °F	±4.0 °F	10 mV/°F	+5 V to +30 V	159 µA
LM35A	Precision Celsius Temperature Sensors	-55 °C to +150 °C	±1.0 °C	10 mV/°C	+4 V to +30 V	133 µA
LM35		-55 °C to +150 °C	±1.5 °C	10 mV/°C	+4 V to +30 V	161 µA
LM35CA		-40 °C to +110 °C	±1.5 °C	10 mV/°C	+4 V to +30 V	116 µA
LM35C		-40 °C to +110 °C	±2.0 °C	10 mV/°C	+4 V to +30 V	141 µA
LM35D		0 °C to +100 °C	±2.0 °C	10 mV/°C	+4 V to +30 V	141 µA
LM45B	SOT-23, Celsius Temperature Sensors	-20 °C to +100 °C	±3.0 °C	10 mV/°C	+4 V to +10 V	160 µA
LM45C		-40 °C to +125 °C	±4 °C	10 mV/°C	+4 V to +10 V	160 µA
LM50B	SOT-23, Single Supply, Celsius Temperature Sensors	-20 °C to +100 °C	±3.0 °C	10 mV/°C	+4.5 V to +10 V	180 µA
LM50C		-40 °C to +125 °C	±4.0 °C	10 mV/°C	+4.5 V to +10 V	180 µA
LM60B	2.7 V, SOT-23, Single Supply Celsius Temperature Sensors	-25 °C to +85 °C	±3.0 °C	6.25 mV/°C	+2.7 V to +10 V	125 µA
LM60C		-40 °C to +125 °C	±4.0 °C	6.25 mV/°C	+2.7 V to +10 V	125 µA
LM61B		-25 °C to +125 °C	±3.0 °C	10 mV/°C	+2.7 V to +10 V	140 µA
LM61C		-40 °C to +125 °C	±4.0 °C	10 mV/°C	+2.7 V to +10 V	140 µA
LM62B		-20 °C to +85 °C	±3.0 °C	15 mV/°C	+2.7 V to +10 V	180 µA
LM62C		-20 °C to +85 °C	±4.0 °C	15 mV/°C	+2.7 V to +10 V	180 µA
DIGITAL OUTPUT						
LM56B	Low Power Thermostats	-40 °C to +125 °C	±3.0 °C	6.2 mV/°C	+2.7 V to +10 V	230 µA
LM56C		-40 °C to +125 °C	±4.0 °C	6.2 mV/°C	+2.7 V to +10 V	230 µA
LM74	SPI/MICROWIRE Temperature Sensor	-40 °C to +125 °C	±1.25 °C	0.0625 °C/LSB	+3.0 V to +5.5 V	1 mA
LM75	I2C Temperature Sensor	-40 °C to +125 °C	±3.0 °C	0.5 °C/LSB	+3.0 V to +5.5 V	1 mA
LM76	12-bit Plus Sign I2C Temperature Sensor	-40 °C to +125 °C	±1.5 °C	0.0625 °C/LSB	+3.0 V to +5.5 V	1 mA
LM77	I2C ACPI Temperature Sensor	-40 °C to +125 °C	±1.5 °C	0.5 °C/LSB	+3.0 V to +5.5 V	1 mA
LM84	SMBus Remote Diode Temperature Sensor	-40 °C to +125 °C	±2.0 °C	1 °C/LSB	+3.0 V to +5.5 V	1 mA
SYSTEM HARDWARE MONITORS						
LM78	ISA Bus / I2C Bus System Hardware Monitors	-40 °C to +125 °C	±3.0 °C	1 °C/LSB	+4.25 V to +5.75 V	1 mA
LM79		-40 °C to +125 °C	±3.0 °C	1 °C/LSB	+4.25 V to +5.75 V	2 mA
LM80	I2C System Hardware Monitor	-20 °C to +125 °C	±3.0 °C	0.0625 °C/LSB	+3.0 V to +5.5 V	2 mA
LM81	SMBus System Hardware Monitor (D/A Output)	-30 °C to +125 °C	±3.0 °C	0.0625 °C/LSB	+2.8 V to +3.8 V	2 mA

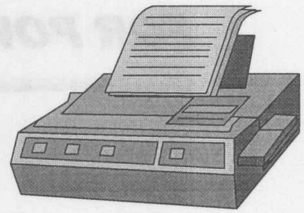
National Semiconductor

ANALOG SOLUTIONS FOR POWER MANAGEMENT

SIMPLE SWITCHER DC/DC Converters for Line-Powered Equipment

- **Simple to design-in**
- **Guaranteed system specifications**
- **Few external components**
- **Standard magnetics**
- **Software support**





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Analog Solutions 2

Most equipment used in the office or home draws its power from the AC line. This line may be between 90 - 264VAC and 47 - 63Hz, depending on which part of the world the equipment is located. However, the internal circuitry and motors rarely operate at these voltages. It now becomes necessary to provide Power Conversion within the equipment. This conversion usually means a power supply using a line transformer plus DC/DC voltage converters.

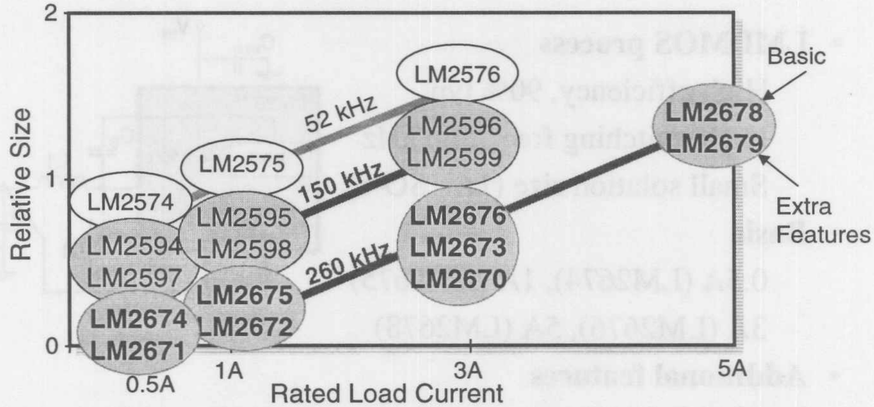
While there are many types of DC/DC voltage converters on the market, there are few that combine the ease-of-use and adaptability of the SIMPLE SWITCHER DC/DC converters.

SIMPLE SWITCHER products offer guaranteed complete supply system performance, such as maximum output voltage tolerance, and not just the tolerance of the subsection of the integrated circuit.

In addition, a SIMPLE SWITCHER is easy to configure, with a variety of standard output voltages available. A few external components are required, and they are fully specified in the product documentation. Components that may be unfamiliar to the system designer, such as inductors, are available as standard part numbers from other vendors.

Design software is also available to custom design a SIMPLE SWITCHER converter for a specific application, complete with recommended external components.

New Step-Down Regulators Add to SIMPLE SWITCHER Line



Output voltage options: 3.3V, 5V, 12V, Adj

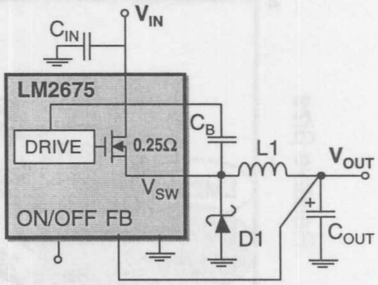
Two new families of step-down (buck) converters have been added to the SIMPLE SWITCHER converter line. The LM259x series is a full line of step-down switching regulators, with three load current ranges including up to 3A. For each load current range, there is a "basic" and a "full-featured" version. The basic regulators offer a complete power converter solution (when used with the four external components specified in the datasheet or design-in software). Additional functions are available with the full-featured products, which allow further power supply design flexibility. The LM259x converters are similar to the earlier LM257x, but with a notable difference in switching frequency (150 kHz vs. 52 kHz for the LM257x).

Another series is newly available, the LM267x. With a higher switching frequency of 260 kHz and very high efficiency of typically 90%, these converters can increase the density of the complete DC/DC converter by a factor of 3:1, compared to the LM257x series.

This discussion will focus on the LM259x series first, then the LM267x converters.

New LM267X Step-Down Simple Switchers

- **LMDMOS process**
  - High efficiency, 90% typ.
  - High switching freq., 260 kHz
  - Small solution size (1A: SO-8)
- **Basic**
  - 0.5A (LM2674), 1A (LM2675)
  - 3A (LM2676), 5A (LM2678)
- **Additional features**
  - LM2670/1/2: Soft-start, Frequency synchronization
  - LM2673, LM2679: Adjustable current limit



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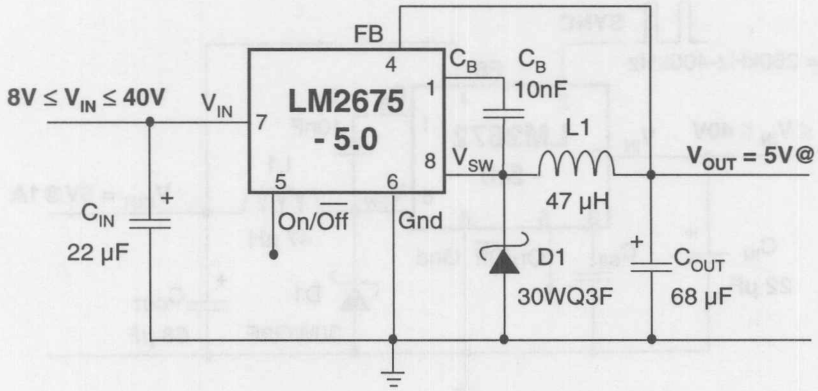
The LM2674 and LM2675 are fully integrated, easy-to-use, high efficiency, DC/DC converters used to accomplish on-board power conversion in a simple and cost-effective manner. These devices have been optimized for ease-of-use, high efficiency and small solution space by use of advanced LMDMOS process, high switching frequency, and smallest packaging. LMDMOS process increases efficiency by minimizing $R_{DS(ON)}$ losses, and higher switching frequency enables the use of smaller, lower profile inductors and capacitors.

A primary advantage of the LM2675 family is that LMDMOS technology allows for a 1A switcher in the popular SO-8 surface mount package. Previously, the LM2594 bipolar converter extended SO-8 capability to 0.5A; the LM2675 now extends this capability to 1A for smallest possible solution space available at that current level. As with all members of the Simple Switcher family, ease-of-use, system specifications, software design tools, and standardized components continue to be fully supported for a total design solution.

The LM2671 and LM2672 switchers offer additional features of softstart and frequency synchronization. All four of the new switchers are offered in the SO-8 and DIP-8 packages.

LM2675: 90% Efficient Step-Down Converter



90% Efficient at V_{IN} = 12V

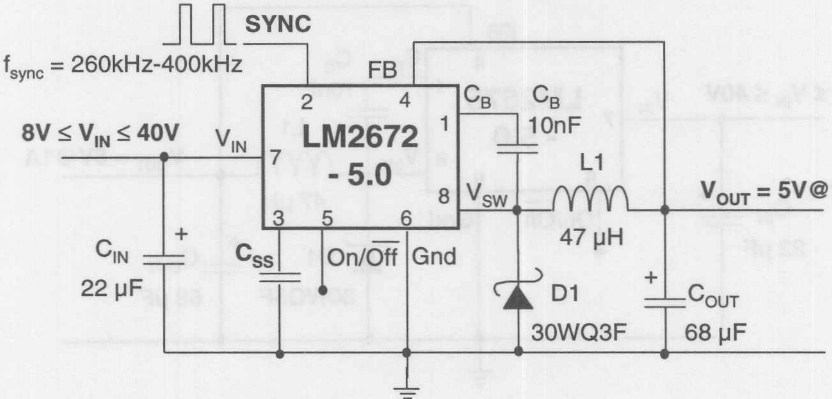
The LM2675 Simple Switcher is typically used as a step-down DC/DC power converter, as in this example.

Compared to other Simple Switcher buck (step-down) converters, there is one small additional component, C_B. This "bootstrap" capacitor, typically 10nF, provides additional gate drive to the internal FET switch for low $R_{DS(ON)}$, which maximizes efficiency. For example, a regulator which converts 12V down to 5V at 1A will yield an efficiency of 90% (typ.). In comparison, a similar design using the bipolar-switch LM2595 will have an efficiency of 82% (typ.), and one using the LM2575 will have an efficiency of typically 77%. LM2675 conversion efficiency is even higher with higher output voltage, typically 96% for conversion from 15V down to 12V at a 1A load. With this higher efficiency, the LM2675 is appropriate for use in portable applications as a battery power converter.

The printed circuit board area required for this converter is minimized because of several features of the LM2675 family. The high efficiency (typically 90% or greater for most applications) will make sure that the part runs much cooler during normal operation compared to the other Simple Switchers, so the small SO-8 or dual-in-line IC package requires very little thermal design of the PC board. The power switch of these regulators operates at 260 kHz, which makes it possible to select and use smaller inductors and capacitors.

As with all Simple Switchers, the system converter specifications are guaranteed. Furthermore, with only five external components needed for the basic designs, the power supply using the LM2675 is easy to design and to use.

LM2672 adds Sync, Soft-Start



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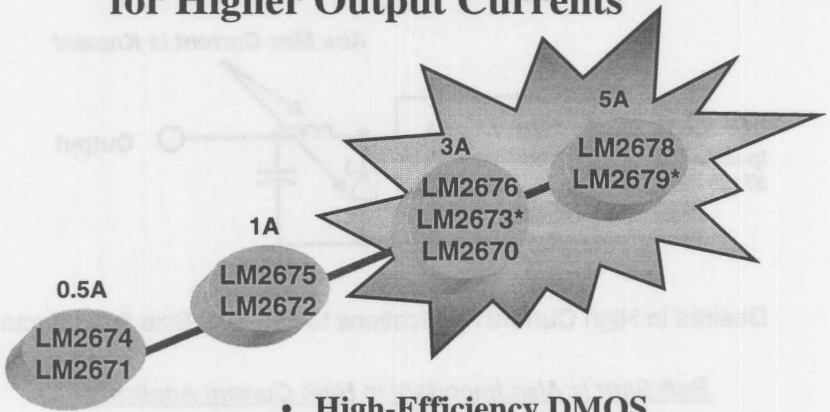
Analog Solutions 6

The full-featured LM2671 and LM2672 are similar to the basic regulators, but offer features for additional flexibility, such as:

The Soft-start feature makes sure that the in-rush current is limited, to avoid overloading the source supply during start-up.

Frequency synchronization makes it possible to run the converter from an external clock with frequencies between 260kHz and 400kHz. By doing this, the system noise and EMI can be reduced because only one frequency (and its subharmonics) need to be filtered. It also makes it possible to shut off the whole system, so allowing a better fault control. With a higher frequency, the components can be smaller.

New "3rd Generation" Simple Switchers for Higher Output Currents

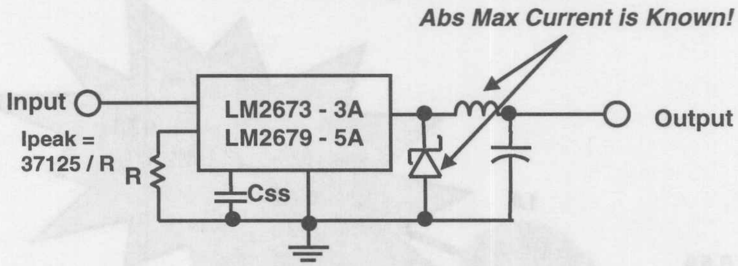


- **High-Efficiency DMOS**
- **Adjustable Current Limit***
- **Soft-Start**
- **Easy to Design!**

Continuing our line of Simple Switcher products, five new products expand the load current capability of our most efficient DMOS switchers to 3A and 5A. Higher efficiency is more important in higher power supplies so the low loss DMOS switch is a plus.

Once again pre-determined component selection is provided to keep designs "simple".

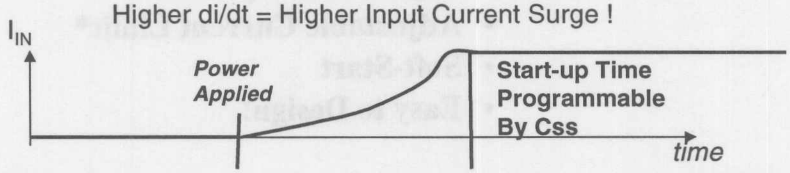
A New Feature... Adjustable Current Limit



Desired in High Current Applications to Properly Size the Inductor

Soft-Start is Also Important in High Current Applications

Higher di/dt = Higher Input Current Surge !



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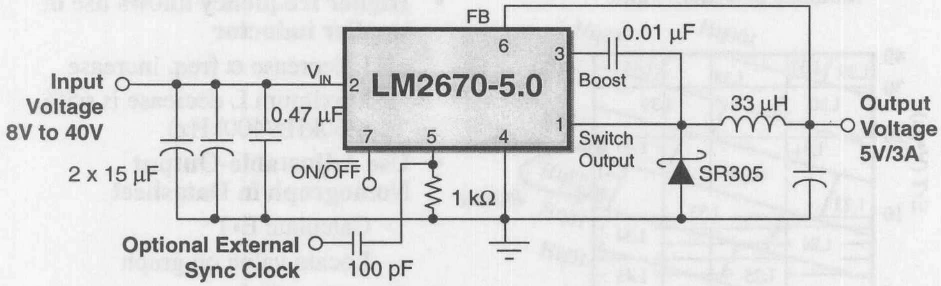
Two key features of these high current devices provide extra protection of the external components and the system in which the regulators are used.

A trend in the switching power supply arena, particularly in high load current applications, is to have switch-mode controllers with an adjustable current limit. The reason for this is to allow system designers to size the inductor and the clamp diode to precisely what is required by the application. Without control of the current limit these components must be rated to handle the maximum current provided by the controller resulting in physically larger sized and possibly more expensive devices than actually required. A single resistor sets up a current source which is compared to a fraction of the DMOS power switch current (by a factor of 37,125) and limits the peak switch current when exceeded.

High current applications also put a bigger demand on the unregulated input voltage source to provide a surge of current at power-on. A soft-start provision has also been included on these new devices. An external capacitor can be connected to restrict the duty cycle and limit the input current demand of the controller for programmable length of time.

3A Buck Simple Switcher Now With Sync



- **Synchronization range is 280 kHz to 400 kHz**
  - Base frequency is 260 kHz
  - Sync to clock minimizes harmonics in system
  - Higher frequency allows use of smaller inductor

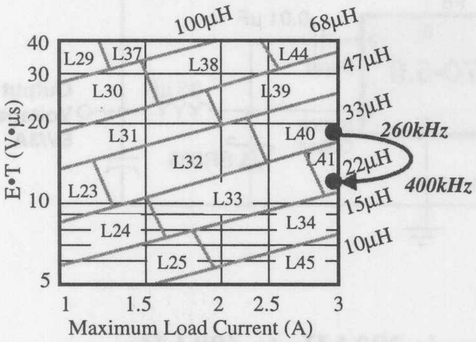
National Semiconductor *Analog Solutions* 9

The 3-Amp LM2670 provides the ability to synchronize the switch to an external clock. The pre-set internal switching frequency is 260kHz. The external SYNC pin allows the user to select a switching frequency anywhere in the range of 280kHz (the upper end of the free-running oscillator frequency) to 400kHz. This allows the use of smaller passive components and reduces output ripple. However, a higher switching frequency will cause the efficiency to be reduced, due to higher switching losses caused by more switching cycles per period of time. After taking this into consideration, the benefit of smaller components may still outweigh the efficiency hit.

Synchronization is also desirable when the frequency of the output ripple is critical in a frequency sensitive system where it could negatively interact with other circuits and functions. Systems with phase-locked loops are a particularly good example. Using synchronization, all the regulators and system clocks can be set to harmonics of the same fundamental frequency. The common noise can then be filtered.

Designing With LM2670

Inductor Selection Guide



Example: $V_{IN}(max) = 40V$, $V_{OUT} = 5V$ @ 3A

$$E\bullet T = \frac{(V_{IN}(max) - V_{OUT} - V_{SAT})(V_{OUT} + V_D)}{V_{IN}(max) - V_{SAT} + V_D} \bullet \frac{1000}{f, kHz}$$

- **Higher frequency allows use of smaller inductor**
  - L decrease α freq. increase
  - Maximum L decrease is 65% (260kHz/400kHz)
- **Use Adjustable-Output Nomograph in Datasheet**
  - Calculate E•T
  - Locate value on graph
- **Capacitor Values**
  - Use standard tables (Tables 3,4,6) to be conservative
  - Use lower values only if stability can be tested
- **Custom frequency not yet supported through software**

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Analog Solutions 10

Selection of external components for the LM2670 operating at a frequency other than the default of 260 kHz requires a calculation and use of the datasheet component tables. In general, the inductor value can be decreased proportional to the increase in switching frequency. At the highest frequency, 400 kHz, the inductor value can be as low as 65% of the 260 kHz value. To find the inductor value, calculate the value for E•T using the equation above. E•T relates to the energy storage required of the inductor. Using the calculated E•T and the maximum load current of the application, identify the inductor value and standard inductor number in the inductor selection guide for the adjustable output voltage product (Figure 6 in the datasheet). In the example above, at the default frequency the inductor value was 33 uH. By increasing the frequency to 400 kHz, the inductor value dropped to 22 uH.

We should be able to decrease the output capacitor value as well, but to do so requires familiarity with power supply design and evaluation, to ensure that the regulator will be stable. A conservative approach is to use the capacitor values recommended by the datasheet in Tables 3, 4, and 6.

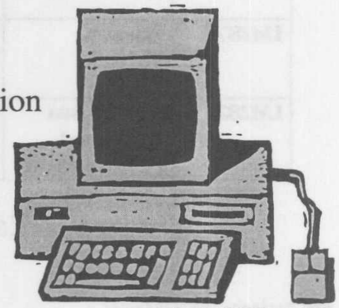
The diode selection does not depend on switching frequency, in the range we are using; Table 5 in the datasheet is appropriate for making the selection.

If the new switching frequency is within about 20% of the default, or less than about 310 kHz, component values can be selected as though the frequency was at the default.

The software "LM267x Made Simple" has not yet been updated to support designs at frequencies other than 260 kHz.

LM267X Made Simple V2.01

- **Windows environment (3.1/95/NT)**
- **Supports newest Simple Switchers, the LM267X high-efficiency step-down converters**
- **Same approach as Switchers Made Simple**
  - Complete design from V_{IN}, V_{OUT}, I_{LOAD}
  - Components fully specified
- **Added features**
  - Variable operating point evaluation
  - Save schematic, design details



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Analog Solutions 11

As a design aid for the LM267X family of Simple Switchers, the software "LM267X Made Simple" (version 2.01) is available. In the tradition of "Switchers Made Simple," "LM267X Made Simple" automates the design of high-efficiency step-down converters. A Windows application, it is even more easy, more flexible and more user friendly compared to the earlier DOS-environment software tools.

"LM267X Made Simple" includes all LM267x Simple Switchers :

LM2671/74 0.5A output step-down converters

LM2672/75 1A output step-down converters

LM2670/3/6 3A output step-down converters

LM2678/9 5A output step-down converters

New SIMPLE SWITCHER Converters Summary

Product Family	Converter Type	Current Ratings	Switching Frequency	Features (*Selected products)
LM267X	Step-Down (Buck)	0.5A, 1A, 3A, 5A	260 kHz	Synchronization* Softstart* Adjustable Current Limit*
LM259X	Step-Down (Buck)	0.5A, 1A, 3A	150 kHz	On/Off Error flag with delay* Softstart*
LM287X	Boost/ Flyback	3A, 5A (switch)	100 kHz	Synch./Freq. Adj.* On/Off*
LM2825	Step-Down Integrated Power Supply	1A	150 kHz	On/Off Softstart

All available in 3.3V, 5V, 12V, and ADJ output options

National Semiconductor   Analog Solutions 12

The newest SIMPLE SWITCHERs from National are noted above. These products extend the capability of the SIMPLE SWITCHER family, to higher output power, higher switching frequency, and additional control features.

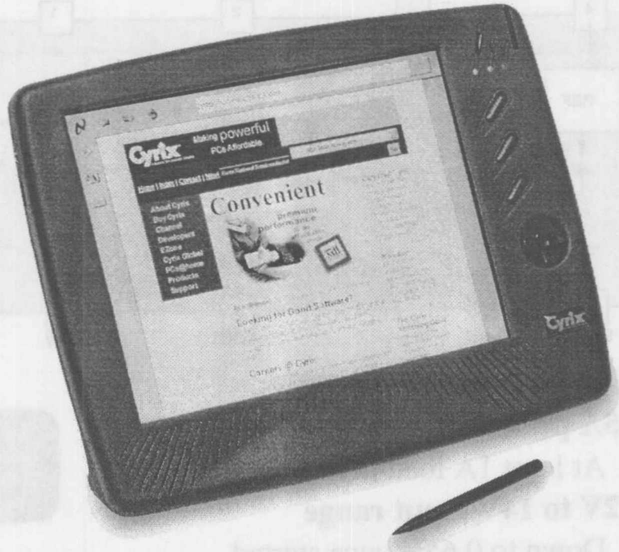
ORIGINAL SIMPLE SWITCHER DC/DC Converter Products

Part Number	Current Rating	Switching Frequency	Features
Flyback			
LM2577	3A (switch)	52 kHz	
Step-Down			
LM2574	0.5A	52 kHz	Shutdown
LM2575	1A	52 kHz	Shutdown
LM2576	3A	52 kHz	Shutdown

Design-in software is available (from the National web site or by request to a National sales office) for all the SIMPLE SWITCHER products requiring external components:

Product(s)	Software
LM267X Family	"LM267x Made Simple" V2.01
LM259X Family	"Switchers Made Simple" V4.3
LM258X Family	"Switchers Made Simple" V4.3
LM2574/5/6/7 Products	"Switchers Made Simple" V3.3

Power Conversion in Portable Electronics



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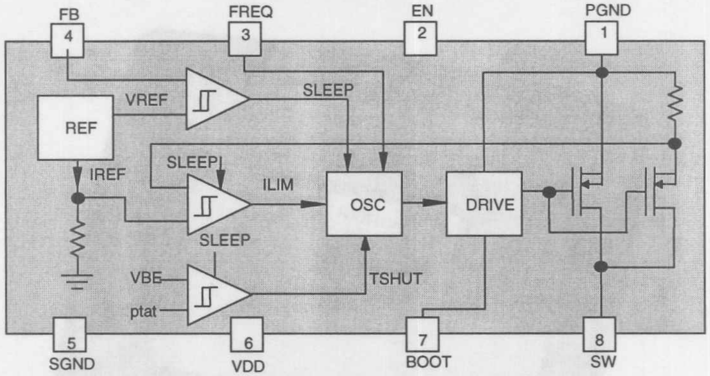
Analog Solutions 13

The WebPAD™ is a portable information appliance. It makes browsing the internet convenient no matter where you are in and around the house or office. But users are unlikely to trade too much performance or too many features solely for the sake of convenience. There in lies one challenge for the designers of portable electronic devices whether they are designing a consumer product like the WebPAD, a high-end cellular telephone for business users, or the bar-code readers used by Federal Express drivers. And in many ways, meeting the challenge involves getting the most out of the battery pack. Inefficient power conversion means less run time or scaling back on processor performance for example.

This section contains information about power conversion products and techniques developed specifically for application in portable electronic devices.

LM2621 "Micro-Boost"



- **High efficiency, up to 90%**
- **2.5A peak switch current**
  - At least 1A load in most applications
- **1.2V to 14V input range**
  - Down to 0.65V once started

National Semiconductor

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The LM2621 is a high efficiency, step-up DC-DC switching regulator for battery-powered and low input voltage systems. It accepts an input voltage between 1.2V to 14V and converts it into a regulated output voltage in the range of 1.24V and 14V. Once started, the LM2621 will remain operational down to an input of 0.65V.

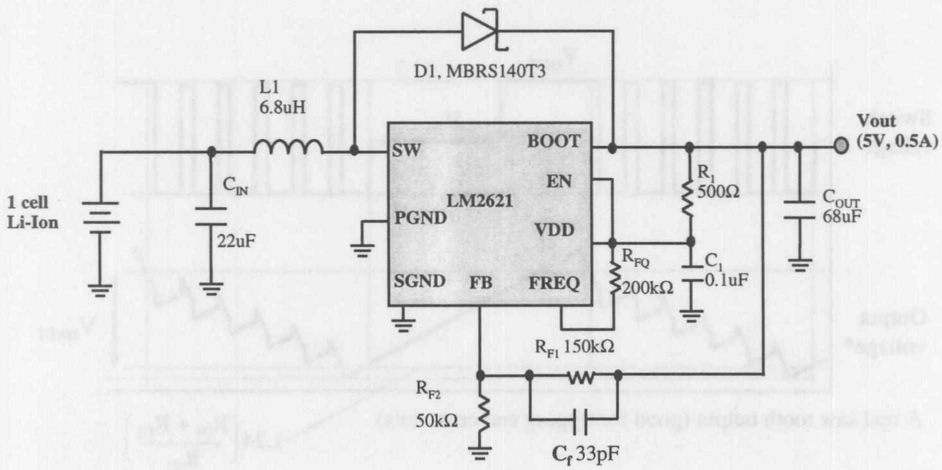
The high switching frequency (adjustable up to 2MHz) of the LM2621 allows for tiny surface mount inductors and capacitors. Because of the unique constant-duty-cycle gated oscillator topology very high efficiencies are realized over a wide range load range. The supply current is reduced to 80µA because of BiCMOS process technology. In the shutdown mode, the supply current is less than 2.5µA.

With its internal 0.17Ω N-Channel FET power switch and gated oscillator approach, efficiencies up to 90% are achievable using the LM2621.

The LM2621 is available in an Mini-SO-8 package. This package uses half the board area of a standard 8-pin SO8 and has a height of just 1.09mm. Combined with the unusually small inductor and capacitor needed in the application, an LM2621 regulation solution usually requires less than half the board area of traditional solutions.

The power switch of the LM2621 is connected to ground which makes it easy to configure as a flyback (buck/boost) converter as well as a step-up (boost) converter.

LM2621 Ideal for Boosting Li-Ion Battery



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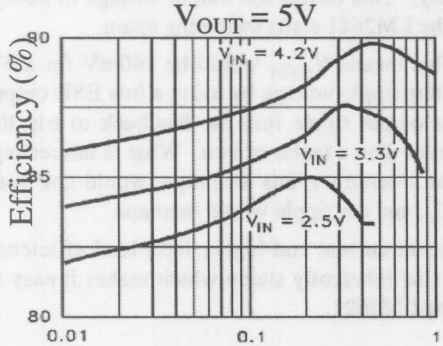
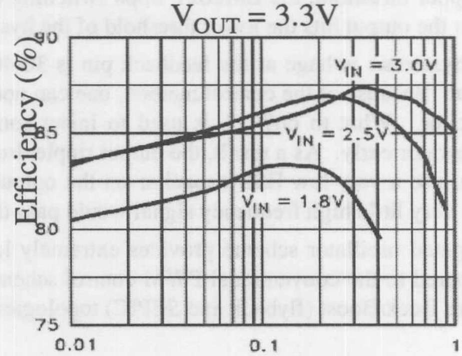
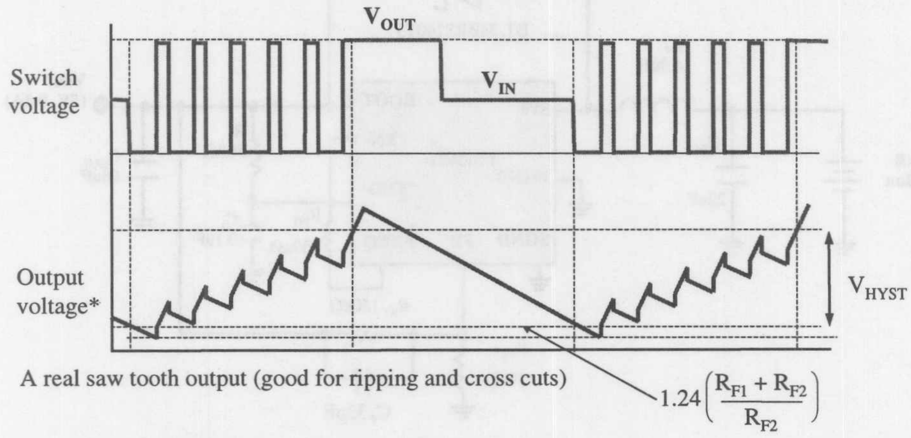
A typical application of the LM2621 converts a 1cell Li-Ion Battery input to a 5V @0.5A output. The high switching frequency allows use of the extremely small DT1608 Coilcraft inductor. The gated oscillator approach provides low quiescent current and high efficiency, typically 87% for this design.

Operating power for the LM2621 comes from the VDD pin. Its operating range is 2.5V to 5.0V. If the output voltage is in that range, as is the case in this example, VDD can be connected to the output via an R-C filter network.





LM2621 Uses Gated Oscillator



* The output ripple is reduced by adding C_f

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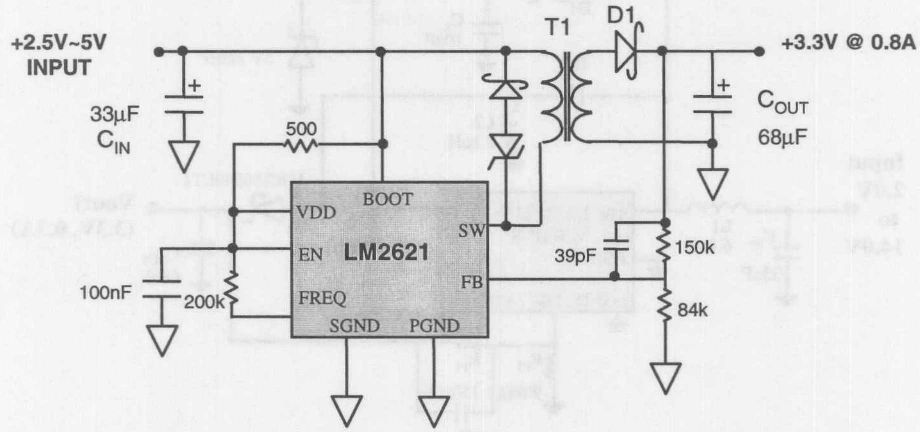
Analog Solutions 16

The gated oscillator control scheme uses a hysteresis window to regulate the output voltage. When the output voltage is below the upper threshold of the window, the LM2621 switches continuously with a fixed duty cycle of 70% at the switching frequency selected by the user. During the first part of each switching cycle, the internal N-Channel MOSFET is turned on. Current in the inductor ramps up and energy is stored in the inductor. During the second part of each switching cycle, the MOSFET is turned off. The voltage across the inductor reverses and current flows through the diode to the output capacitor and the load. LM2621 switches continuously and the output continues to ramp up. When the output hits the upper threshold, the LM2621 stops switching completely. This causes the output voltage to decay. When the output hits the lower threshold of the hysteresis, the LM2621 starts switching again.

The hysteresis voltage at the feedback pin is 30-40mV. This means V_{HYST} would be 160mV for a 5V output. Because of the control method, one can not reduce this ripple voltage by using a low ESR output capacitor. What to do? C_f is used to inject some of the output ripple into the feedback to trip the comparator early. As a result, the output ripple drops by better than a factor of two. What is interesting, if you use a very low ESR capacitor on the output (such as a ceramic), this technique would not work since very little high frequency signal would pass through C_f, and the ripple would increase.

The gated oscillator scheme provides extremely low quiescent current and higher light load efficiency compared to the conventional PWM control scheme. It is also inherently stable which makes it easy to realize Buck/Boost (flyback and SEPIC) topologies using the LM2621.

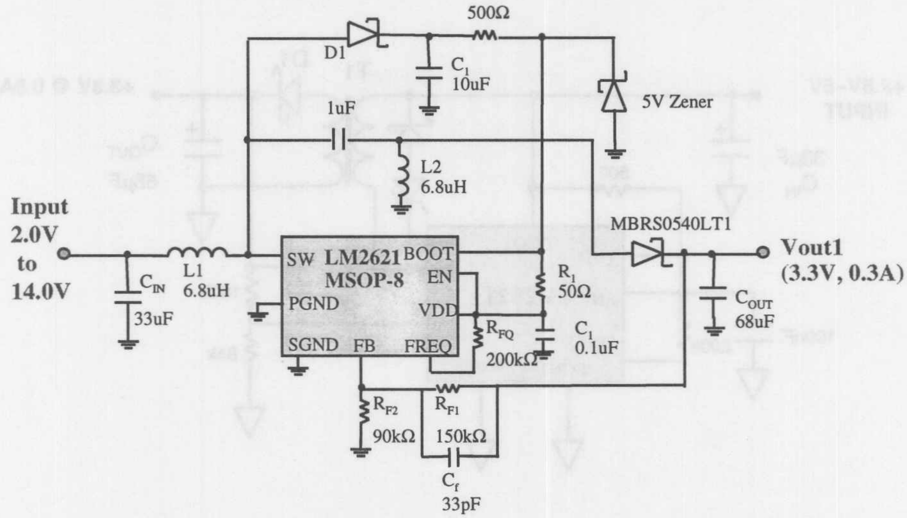
Flyback Converter Delivers 3.3V/0.8A From Wide-Range Input



Here is the LM2621 shown in flyback topology. Because of its gated oscillator operation, no extra components are needed for stabilizing the circuit.

This circuit offers step-up/step-down operation and gives the option of multiple outputs as well as negative outputs.

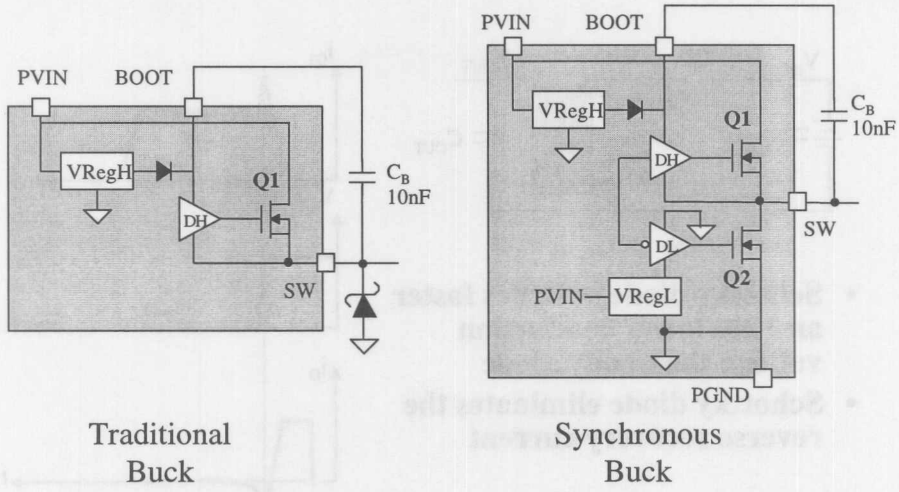
Wide Input Voltage Range SEPIC



This LM2621-based SEPIC regulator takes an input voltages in the range of 2.0V to 14V and provides a 3.3V output at up to 300 mA. A virtual boost circuit (consisting of D1, C1 and the zener) is used to start the SEPIC at low voltages. An LDO can be added at the output of the virtual boost circuit to create a second output.

SEPIC: Single Ended Primary Inductance Converter

Synchronous Buck Converters Offer Increased Efficiency for Battery-Powered Systems



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Traditionally, a MOSFET and a diode (preferably Schottky diode) are used in the buck converter. For applications like battery powered systems, where high efficiency is critical, another MOSFET is used to replace the diode in synchronous rectification. "Synchronous rectification" means that, instead of having an external diode connected from the SW pin to ground to maintain current flow when the switch Q1 is off, the internal FET Q2 is actively driven during the off-time. The advantage of synchronous rectification is in the lower voltage drop produced by Q2 while it is conducting, compared to that of a diode.

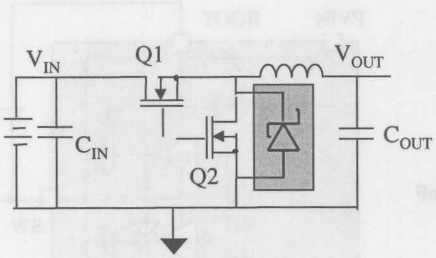
In the case of the LM2650, a synchronous rectifier buck, it has a low $R_{ds(ON)}$ of 125mΩ, so if Q2 is conducting 3A it has a voltage drop of only 375mV. To get an equivalent voltage drop from a diode, a Schottky diode with a 5A rating would be needed. In addition, since Q2 is actively driven, it turns on much more quickly than a diode would, reducing power loss during the switch transition.

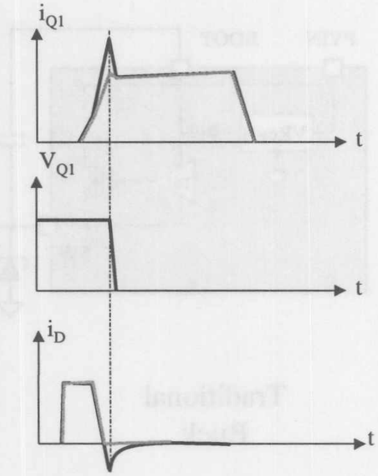
Q1 and Q2, the output switches, are controlled by the drivers DH and DL (respectively). There is a 50ns delay between one switch beginning to turn off and the other switch beginning to turn on, which prevents the switches from conducting at the same time, and therefore prevents current from "shooting through" directly from the input supply to ground.

As Q1 turns on, its source voltage swings up to just below the input voltage. The LM2650 uses a "bootstrapping" technique to pull the positive supply of DH up, along with the source voltage of Q1, to a voltage above the input voltage. Because the source of Q1 and the positive supply of DH make the same voltage swing together, DH maintains the positive gate-to-source voltage required to turn Q1 on. Q1 plays an active role in pulling the supply of DH up, and is therefore said to pull itself up by its "bootstraps", thus the name of the technique and of the BOOT pin.

In a typical application, a capacitor CB is connected externally between the BOOT and SW pins. When Q2 is on, the input supply charges CB through VRegH and the internal diode D.

Additional Schottky Diode Further Improves Efficiency





- **Schottky diode switches faster and has lower conduction voltage than body diode**
- **Schottky diode eliminates the reverse recovery current**

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An Schottky diode can be added in parallel with the low-side MOSFET to further improve the efficiency:

(1) Reduce the conduction loss during deadtime by avoiding turning on the body-diode of Q2.

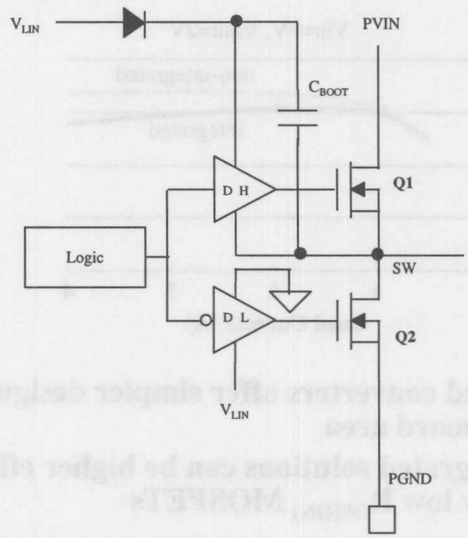
(2) Reduce the Q1 turn-on current spike by eliminating the reverse-recovery current associated with turning off the body-diode (illustrated as above). Since the voltage across Q1 is still high when the current spike appears, the Schottky diode also reduces the switching loss in Q1.

(3) Eliminate the reverse-recovery loss in the body-diode of Q2.

For IC with MOSFETs integrated, the reduction of losses also helps to reduce the power dissipation in the IC.

For layout consideration, the Schottky diode needs to be placed as close to Q2 as possible. The parasitic inductance in the loop of the Schottky diode and Q2 will delay the turn on of the Schottky diode. Devices with the Schottky diode and MOSFET in the same package are also available.

Boost Supply for High-Side Gate-Driver



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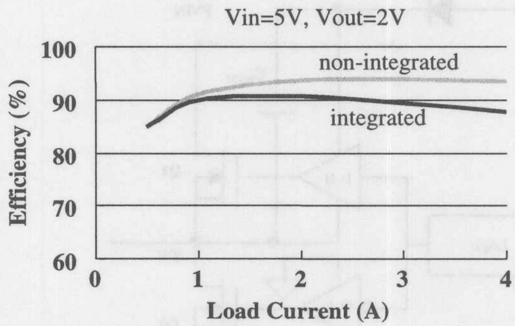
Analog Solutions 21

N-channel MOSFETs are often used in circuits to minimize the $R_{DS(ON)}$. For a given die size and breakdown voltage, an n-channel device has about half of the $R_{DS(ON)}$ of a p-channel device.

When the high-side MOSFET is on, its source is pulled up to the input voltage. To properly drive the gate above the source, a boost circuitry is needed for its driver. In the above diagram, the voltage across CBOOT is charged up to V_{LIN} minus one diode drop when Q2 is on. When Q1 is turning on, CBOOT is providing the boosted gate to source voltage.

This technique is also used for non-synchronous buck regulators using an N-channel MOSFET switch, such as the LM267x high-efficiency Simple Switcher converters.

Integrated (with MOSFETs) vs Non-integrated: Both are Valid Choices

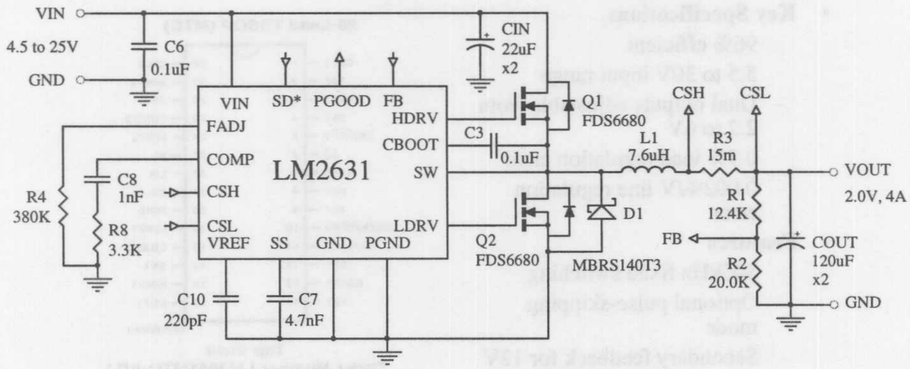


- **Integrated converters offer simpler designs, smaller board area**
- **Non-integrated solutions can be higher efficiency with very low $R_{DS(ON)}$ MOSFETs**

National provides both buck switching regulators (with MOSFETs integrated in the IC) and buck switching controllers (external MOSFETs).

When making choices between using integrated and non-integrated devices, one important criterion is the current requirement. Since the discrete MOSFETs have bigger die area, the on-resistance is usually lower than integrated solution. Therefore, converters using discrete MOSFETs tend to have higher efficiency when load current is higher. On the other hand, integrated devices provide simpler designs and cost and board size savings.

LM2631 Step-Down Controller for Processor Core Supply



The LM2631 provides all the active functions for step-down (buck) switching converters. These DC/DC converters provide CPU core power in battery-operated systems.

Synchronous rectification and pulse-skipping at light loads provide high-efficiency over a wide load range. Bootstrapping of the high-side gate driver allows application of high-side N-channel power MOSFETs for lowest system cost without the need for an external gate-drive voltage higher than that of the high-power input.

Current mode control and high DC loop gain provide excellent line regulation (typically 0.002%V), load regulation (typically 0.3% over the entire load range), and fast response to line and load transients. Current mode control also provides cycle-by-cycle current limiting.

The switching frequency is internally fixed at 200Khz and can be adjusted upwards to as high as 400KHz using a single external resistor. Logic inputs can be used to shut the device down and reduce quiescent current to 0.1µA (typical), override the pulse-skipping mode and keep the LM2631 in fixed-frequency PWM operation regardless of the load current level, and synchronize the switching frequency with an external clock signal. A logic output flag indicates the state of the output voltage.

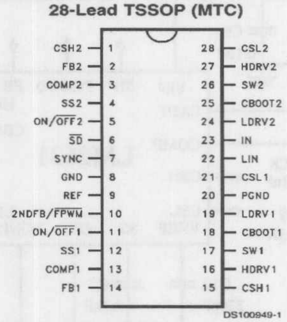
Protection circuitry includes thermal shutdown, output undervoltage and overvoltage shutdown, soft start, and two levels of current limiting (the first level is direct cycle-by-cycle limiting, and the second is a complete shut down of operation if the load pulls the output voltage lower than 80% of the target regulation voltage).

Features include: 4.5 to 30V input range, 1.5 to 6V output range, 200 to 400KHz adjustable switching frequency, synchronization with an external clock signal, precision 1.24V reference output, 0.8 mA typical quiescent current, 0.1µA typical shutdown current, thermal shutdown, cycle-by-cycle current limiting, input undervoltage lockout, output undervoltage and overvoltage shutdown, programmable soft start, and availability in a tiny 20-lead TSSOP.

LM2641 Dual Step-Down Controller for System 5V and 3.3V Supplies

- **Key Specifications**
  - 96% efficient
  - 5.5 to 30V input range
  - Dual outputs adjustable from 2.2 to 6V
  - 0.5% load regulation error
  - 0.002%/V line regulation error
- **Features**
  - 300kHz fixed switching
  - Optional pulse-skipping mode
  - Secondary feedback for 12V
  - Precision 2.5V reference out
  - Programmable soft start

28-Lead TSSOP (MTC)



Top View
Order Number LM2641MTC-ADJ
See NS Package Number MTC28

The LM2641 is a dual step-down power supply controller intended for application in notebook personal computers and other battery-powered equipment.

Fixed-frequency synchronous drive of logic-level N-channel power MOSFETs is combined with an optional pulse-skipping mode to achieve ultra efficient power conversion over a 1000:1 load current range. The pulse-skipping mode can be disabled in favor of fixed-frequency operation regardless of the load current level.

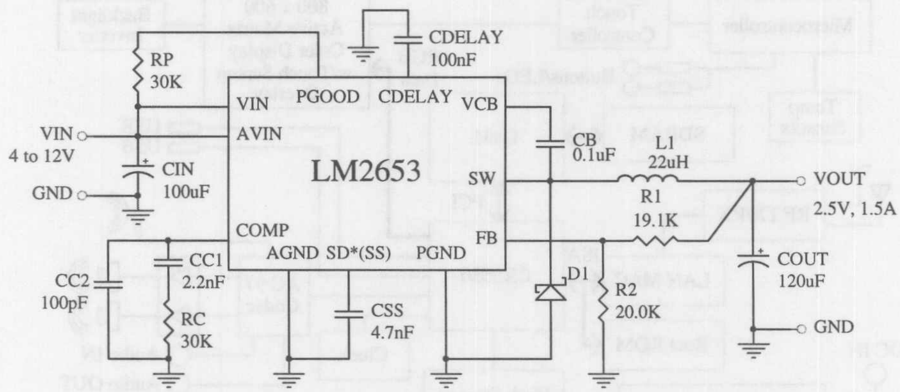
High DC gain and current-mode feedback control assure excellent line and load regulation and a wide loop bandwidth for fast response to dynamic loads.

An internal oscillator fixes the switching frequency at 300kHz. Optionally, switching can be synchronized to an external clock running as fast as 400kHz.

An optional soft-start feature limits current surges from the input power supply at start up and provides a simple means of start up sequencing.

Logic-level inputs allow the switchers to be turned ON and OFF separately.

LM2653 Integrated Synchronous Buck Regulator



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The LM2653 switching regulator provides high efficient power conversion over a 100:1 load range (1.5A to 15mA). This feature makes the LM2653 an ideal fit in battery-powered applications.

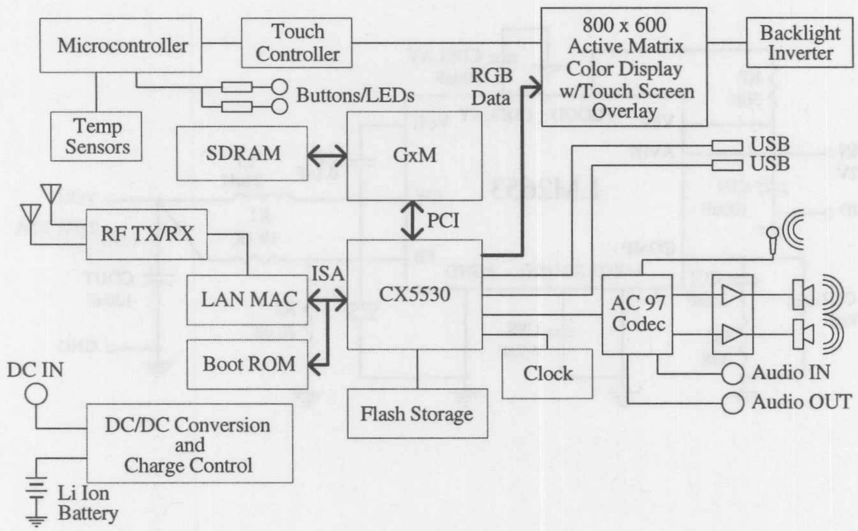
Synchronous rectification is used to achieve up to 97% efficiency. At light loads, the LM2653 enters a low power hysteretic or "sleep" mode to keep the efficiency high. In many applications, the efficiency still exceeds 80% at 15mA load. A shutdown pin is available to disable the LM2653 and reduce the supply current to less than 10uA.

All the power, control, and drive functions are integrated within the ICs. The ICs contain patented current sensing circuitry for current mode control. This feature eliminates the external current sensing resistor required by other current-mode DC-DC converters.

The ICs have a 300kHz fixed frequency internal oscillator. The high oscillator frequency allows the use of extremely small, low profile components.

Protection features include thermal shutdown, input undervoltage lockout, adjustable soft-start, output overvoltage protection, and two levels of current limits: The first level limits the load current on a cycle-by-cycle base; at the second level, if the load pulls the output voltage down below 80% of the regulated value, the chip will latch off.

WebPAD Block Diagram



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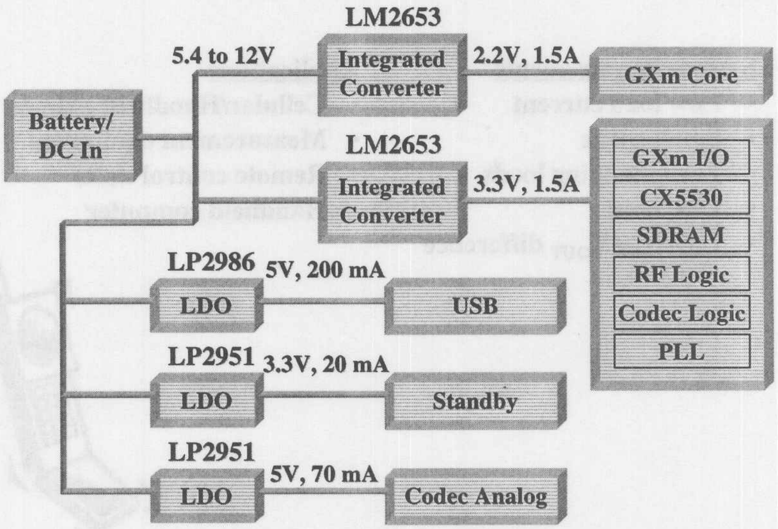
Analog Solutions 26

Returning to our example of the WebPAD, the WebPAD is a portable Internet browser. The MediaGX (GXm) processor provides fast processing (MII core). The large color display and stereo sound system provide a high-quality human interface. RF circuitry provides fast, wireless connectivity. And efficient DC/DC converters provide long battery life. All are required for an enjoyable experience.

WebPAD DC/DC Conversion



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Analog Solutions 27

In the current WebPAD architecture, an LM2653 integrated voltage regulator provides GXm core power, and a second LM2653 provides GXm I/O power and power for the CX5530 GXm companion chip, memory and other logic. Low-dropout linear voltage regulators (LDOs) provide power for the remaining circuitry. All in all, the DC/DC conversion must be efficient and inexpensive, and this is handled quiet nicely with a mix of switchers and linear regulators. Note, this diagram is simplified. Also note, 200 mA total is a peak load for the USB regulator, 40 mA is typical. Using LDOs for both 5V supplies allows running each Li Ion cell down to 2.7V. Applying standard linear voltage regulators having dropouts in the 1.5 to 2.0V range would require stacking at least three Li Ion cells.

Low-Dropout (LDO) Regulators

System Requirements
- **Low load current**
- **Small space**
- **Fast-changing loads**
- **Low noise**
- **Low V_{IN}-V_{OUT} difference**

Applications
- **Cellular/Handheld phones**
- **Measurement equipment**
- **Remote control units**
- **Handheld computer**

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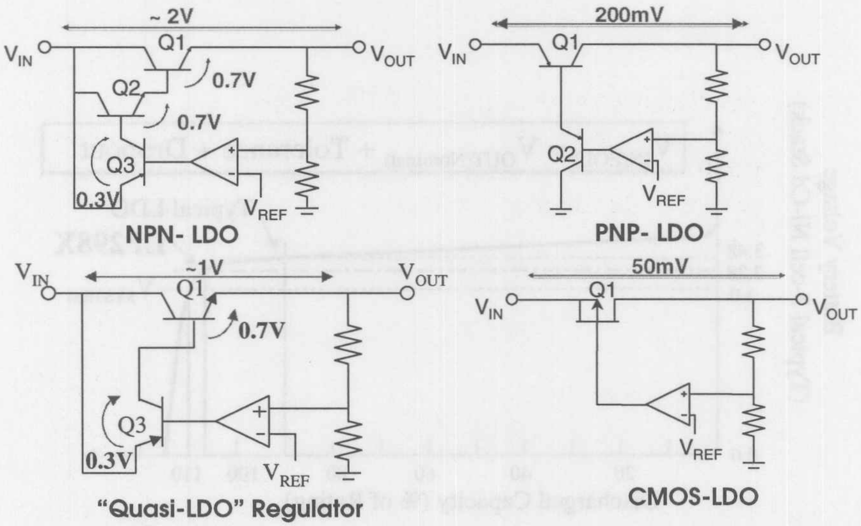
When developing the power conversion solution for a battery-powered system, there are generally three key considerations: Maximizing battery life, providing the necessary system voltage, and minimizing solution size.

To maximize battery life, the power conversion must be done at a high efficiency, so the least possible amount of battery power is wasted. In addition, the converters should have standby or shutdown modes in which no more than a few microamps are drawn.

To provide the required system voltage(s), it may necessary to step up the battery voltage, or step down, or some combination of the two. The choice of topology will also depend on the type of battery cells used (and their voltages at full charge and end of life), and the number of cells in a stack.

The power conversion solution size can be minimized by choosing products with the highest integration in the smallest packages. Sometimes the best choice is a simple, single regulator in a tiny package; alternatively, a highly-integrated switching regulator in a larger surface-mount package may be best. This choice depends on the physical size of the PC boards in the unit, and the flexibility of component placement.

Drop-Out Voltage...



Lower Drop Out Voltage: Longer Battery Life, More Efficient Operation

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Analog Solutions 29

Dropout voltage is the minimum input to output voltage differential required for the regulator to sustain an output voltage within 100mV of it's nominal value.

Use of an NPN power transistor requires more than 1V of drop-out mainly due to the need to provide at least 0.6V to forward bias a base emitter junction. LDO (Low Drop-Out) regulators on the other hand use a PNP for the power transistor. This PNP is allowed to saturate and thereby requires much less drop-out voltage. Newer developments using a CMOS power transistor can provide the lowest drop-out voltage. With CMOS the only voltage drop across the regulator is the ON resistance of the power device times the load current. With very light loads this can become just a few tens of millivolts.

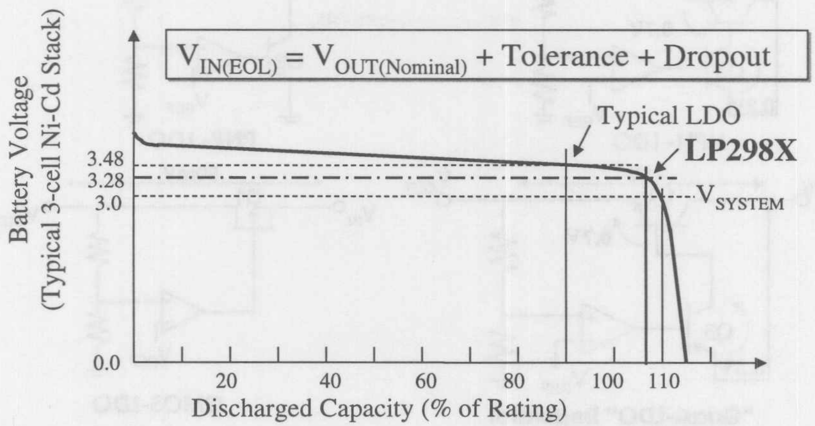
The Quasi-LDO fits between the standard NPN regulator and the PNP-based low-dropout (LDO) regulator, in terms of regulation performance and dropout voltage. The key difference between the three types of regulator is the pass transistor configuration.

The NPN regulator uses an NPN-Darlington driven by a PNP as its pass device. This requires very little drive current from the error amplifier to handle a large load current, but it constrains the minimum voltage drop from input to output.

The PNP-based LDO has a simpler pass device, consisting of one PNP driven by a second lower-current PNP. The dropout voltage is only one V_{BE}, about 0.6V. However, a much higher operating current is needed in proportion to the load.

A quasi-LDO regulator uses an NPN as the main pass transistor, driven by a PNP. As the NPN usually has more current gain than does a PNP, this gives the regulator more gain compared to the traditional LDO, and therefore better load regulation - but not as good as the standard NPN regulator. But with only one NPN instead of a Darlington in the pass device, the quasi-LDO has a lower dropout, a V_{CE}(sat) plus a V_{BE}, or about 1V. Operating current for the quasi-LDO will be lower than for an LDO, but generally not as low as for an NPN regulator.

Maximize System Run-time with Precision LDOs



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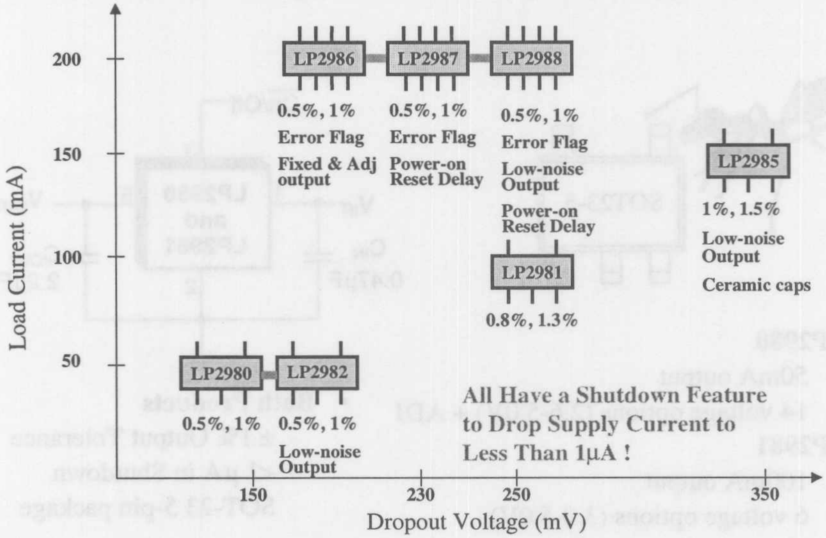
Analog Solutions 30

Minimizing drop-out voltage becomes most beneficial in battery powered systems. The lower the supply battery is allowed to discharge before the system loses properly regulated operating voltages translates directly into increased run time on a single battery charge.

Shown here, use of a regulator with a low enough dropout voltage can allow the battery to discharge beyond its rated discharge capacity before the system operation is effected. This can result in several hours of extra run time.

Precision Bipolar Low Dropout Regulators



National Semiconductor — *Analog Solutions* 31

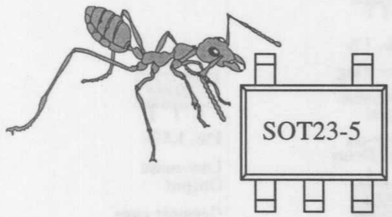
Most battery powered systems also have a requirement for physically small circuitry, Cell phones are a good example.

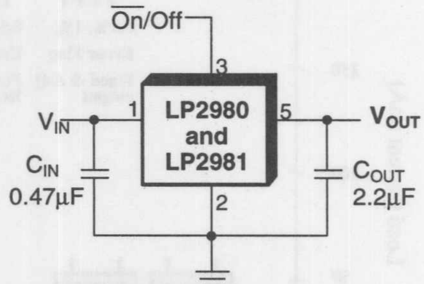
This is an overview of National's LP298X family of LDOs. These regulators are packaged in the smallest footprint allowable for the die size. With current ratings from 50mA to 200mA these regulators are used in very high volumes by small portable electronics manufacturers.

Each regulator in the family is precision trimmed for less than 1% accuracy of the output voltage. This precision not only provides well controlled operation of load circuitry but also gives consistent performance from unit to unit for dropping out of regulation at the end of the battery run time.

Load Current	Part Number	Dropout Voltage	Tolerances Available	Features	Packages
200 mA	LP2986	230 mV	0.5%, 1%	- Fixed & Adj output - 1 µA Shutdown - Error Flag	Mini SO-8, SO-8
	LP2987		0.5%, 1%	- Power-on Reset Delay - 1 µA Shutdown - Error Flag	
	LP2988		0.5%, 1%	- Low-noise Output - Power-on Reset Delay - 1 µA Shutdown - Error Flag	
100 mA	LP2981	250 mV	0.8%, 1.3%	- 1 µA Shutdown	SOT23-5
50 mA	LP2982	150 mV	1%	- Low-noise Output - 1 µA Shutdown	SOT23-5
	LP2980		0.5%, 1%	- 1 µA Shutdown	

Tiny Bias Supply for Light Loads





- **LP2980**
  - 50mA output
  - 14 voltage options (2.6-5.0V) + ADJ
- **LP2981**
  - 100mA output
  - 6 voltage options (3.0-5.0V)
- **Both Products**
  - ± 1% Output Tolerance
  - <1 µA in Shutdown
  - SOT-23 5-pin package

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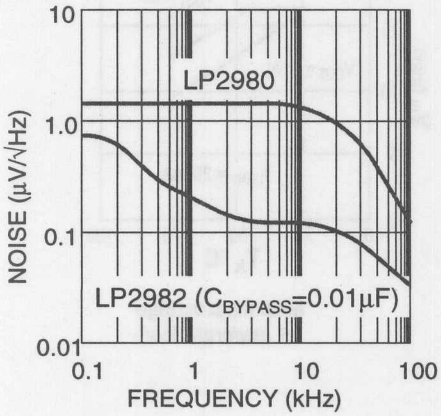
Analog Solutions 32

Using the tiny 5 lead SOT-23 package provides pins to add extra features such as shut down and adjustable output voltage capability. With electronic control of shutdown, the load circuitry and the regulator itself can be automatically shutdown when not needed by the system to draw less then 1uA from the battery supply.

These regulators are also available in several fixed output voltage settings through mask programmability. As the maximum voltage limits of digital circuitry changes due to VLSI and sub-micron processing, these regulators are easily tailored to provide the required voltages.

50mA: LP2980 With Noise Bypass = LP2982
200mA: LP2987 With Noise Bypass = LP2988

Output Noise Density



RMS Noise Comparison

- 300Hz-50kHz bandwidth
- C_{OUT} = 10µF

- **LP2980: 160mV$_{RMS}$**
- **LP2982: 30mV$_{RMS}$**
  - C_{BYPASS}=0.01µF

- **LP2987: 100mV$_{RMS}$**
- **LP2988: 20mV$_{RMS}$**
  - C_{BYPASS}=0.01µF

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Analog Solutions 33

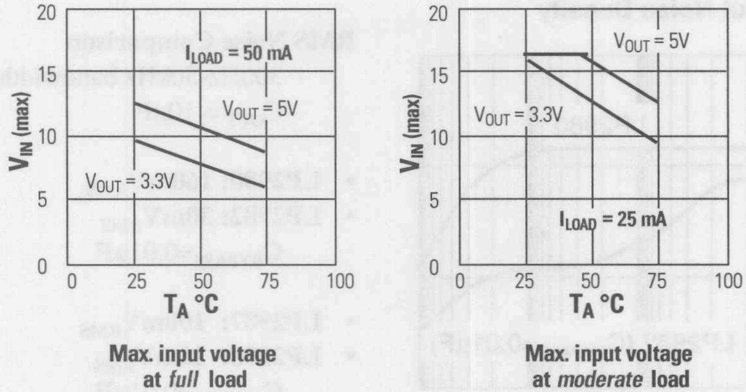
The LP2980 and LP2982 are also a matched set. While the noise of these 50mA regulators is a little higher than that of the 200mA LP2987 and LP2988, the LP2982 receives a similar benefit with the addition of an 0.01µF bypass capacitor.

In the case of both the LP2980/82 and LP2987/88, use of a bypass capacitor reduces the overall output noise by a factor of 5.

All of the LP298x regulators are favored for use in wireless applications, so they needed to be in the smallest possible packages. Increasing the die area further, to reduce noise, would have forced the products into the next-size-larger packages, which was not considered an acceptable solution.

Practical Input Voltage Range

SOT23-5 Thermal Resistance Limits LP2980 Max. Input Voltage



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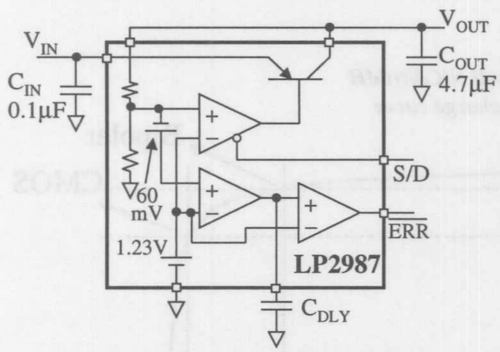
Analog Solutions 34

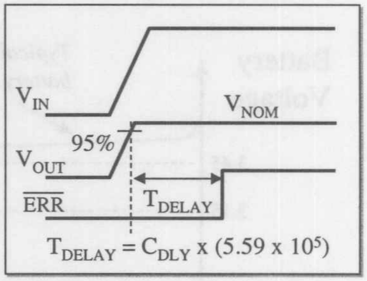
While small packages are advantageous for many reasons, they also come with an inherent limitation. The small physical size does not allow for as much internal power dissipation as larger packages with more thermal mass.

Most of the power dissipated in the regulator is in the power transistor. This power is simply the difference between the input and output voltage times the load current. An easy way to think of controlling the total power dissipation is to control the maximum input voltage for a given load current.

These devices can operate at high input voltages (up to 16V) and can provide a reasonable amount of output current…but not necessarily at the same time…due to power dissipation restrictions.

200 mA Ultra-Low Dropout Regulator has Power-On Reset





- **Three products in family**
  - LP2987 features Power-On Reset Delay
  - LP2988 adds Low-Noise Bypass
  - LP2986 omits POR, adds output adjustability
- **All: 180 mV dropout at full load, 230 mV max**

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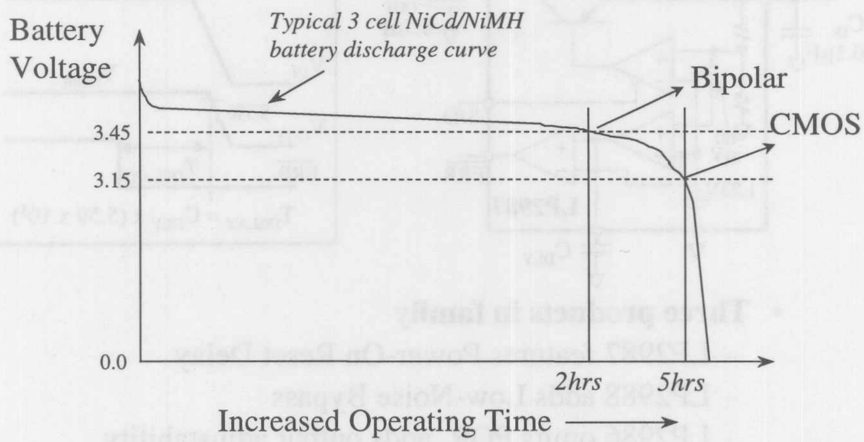
Analog Solutions 35

To obtain higher current operation and yet maintain very low drop-out voltage performance, the 200mA family of regulators required a larger die size. The larger die is packaged in the Mini-SO-8 package which results again in the ability to add additional features for the extra available pins.

In addition to the standard shutdown capability, other features available on the different devices include a delayed power on reset (POR), low noise bypassing and ability to adjust the output voltage.

Operating from reduced battery voltage extends system run-time



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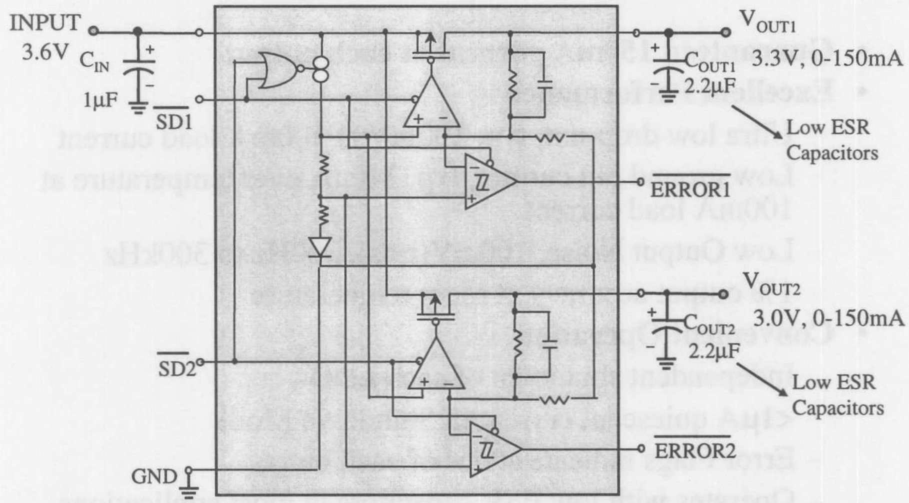
Analog Solutions 36

Once again, lower dropout voltage results in longer run time of battery systems. With CMOS power devices resulting in the lowest drop-out characteristic, the simple change in manufacturing technology can produce astounding increases in operating time. This illustrates up to 2.5 times longer life using CMOS for the regulator.

LP2966 Dual 150mA CMOS LDO Regulator



- Low drop-out and low ground current extend battery life

The LP2966 dual CMOS ultra low-dropout regulators operate from a +2.70V to +7.0V input supply and deliver at least 150mA current at each output over the full operating temperature range. The IC operates with extremely low quiescent current which makes it very suitable for battery powered and portable applications. Each LDO in the LP2966 has independent shutdown capability. The LP2966 provides low noise performance with low ground pin current in an extremely small MSOP-8 package. Additionally, a wide range of preset voltage options are available for each output.

The regulators in the LP2966 use a power MOSFET with an ON resistance of only approximately 1Ω. This results in extremely low drop-out requirements, only 100mV for a 100mA load, and even less for lighter load current requirements.

LP2966 150mA Dual
Ultra Low Drop-out Regulator

- **Guaranteed 150mA current at each output**
- **Excellent Performance**
  - Ultra low drop-out, typ. 100mV at 100mA load current
  - Low ground pin current, typ. 340uA over temperature at 100mA load current
  - Low Output Noise, 100mV(rms), 300Hz to 300kHz
  - 1% output accuracy at room temperature
- **Convenient Operation**
  - Independent shutdown of each LDO
  - <1μA quiescent current in Shutdown Mode
  - Error Flags indicate status of each output
  - Operates with low ESR capacitors in most applications
- **Available in MSOP-8 Package**

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Analog Solutions 38

Here is a summary of the key specifications for this new regulator using CMOS technology.

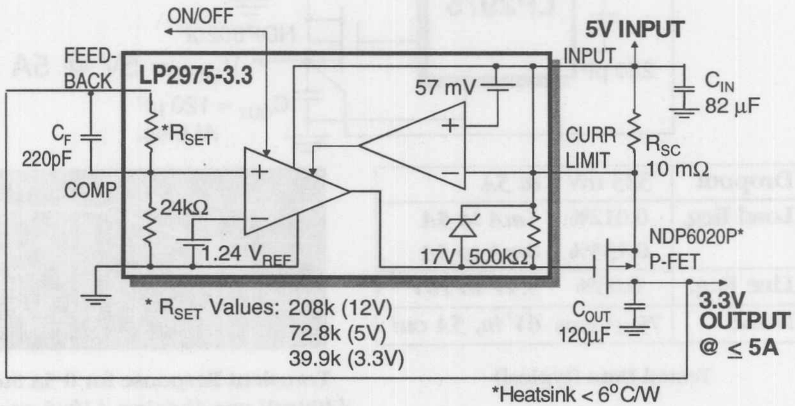
Beside offering the lowest possible drop-out, an equally impressive characteristic is the very low operating current, only several hundred microamps at high load current. The reason for this is that the power MOSFET is a voltage driven device and thus does not require additional base current to provide high output current as is the case with bipolar transistor designs.

One somewhat limiting characteristic of the CMOS implementation is a maximum input voltage restriction to only 7V. This is due to the low voltage CMOS process used for manufacturing the regulator.

Watch for more developments in this exciting technology for voltage regulators to come in the future.

LP2975 P-FET LDO Controller

- **High-Current LDO**
- **Ultra-Low Dropout Regulator**



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There are many low-dropout linear regulator ICs available today that cover the range of <1A output requirements. As the load current rating increases, fewer integrated solutions are available, as they tend to be expensive to integrate, and the number of "standard" requirements goes way down.

For output currents over about 1A, the combination of LDO controller and external pass device gives a more practical, lower-cost solution.

An additional application of a controller-based regulator is to generate an ultra-low dropout supply. By selecting a FET with a low $R_{DS(ON)}$, the input voltage can be allowed to get to within a few tens of millivolts of the regulated output voltage.

The LP2975 LDO controller drives an external P-channel MOSFET to produce an accurately-controlled output voltage. To minimize the solution size, the LP2975 is available in the tiny Micro-8 package (3mm x 5mm). In many applications, surface-mount FETs can also be used.

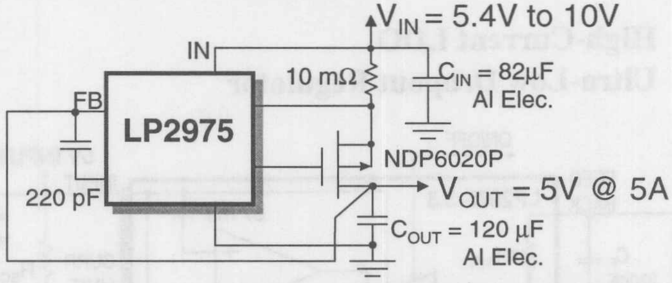
Drawing less than 1 µA in shutdown, the LP2975 can be used in applications requiring a low-power shutdown mode. In normal operation, the LP2975 still has a low supply current of less than 320 µA.

Standard output voltage settings of 12V, 5V, and 3.3V are available, with tolerances of 1.5% or 2.5%. In addition, each part also has adjustment control of the output voltage, using two external divider resistors. Minimum output voltage is 1.24V (the level of the internal reference).

As the P-FET pass device is external to the regulator IC, current limit must also be partly external. The LP2975 has a built-in current limit amplifier, with a 57 mV (typ.) threshold, which can be used to detect the P-FET current passing through a current limit resistor R_{SC}.

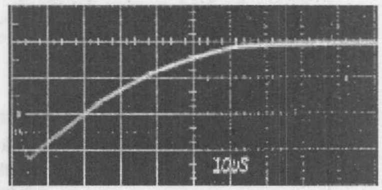
The typical application shown here includes all components needed to create a complete 5A regulator.

Design Example: High-Current LDO



Dropout	**323 mV**	***at 5A***
Load Reg.	**0.012%**	***5mA to 5A***
	0.135%	***0mA to 5A***
Line Reg.	**0.03%**	***5.4V to 10V***
Noise	**75 µVrms**	***6V in, 5A out***

Tested Data (typical)



Transient Response for 0-5A Step (200mV per division / 10µS per div)

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Analog Solutions 40

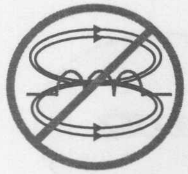
To handle a large output current, such as 5A, and to have a low dropout voltage, the MOSFET needs to have an appropriately high current rating. The NDP6020P is rated for 35A with an $R_{DS(ON)}$ of less than 0.028Ω for V_{GS} of 0.27V. This needs to be a through-hole device, in a TO-220 package, as the FET must be heat-sunk to keep its internal temperature below its rating at full load. The heat sink must be 1.5°C/W if the FET is to survive a short-circuit with $V_{IN} < 7V$, or 6°C/W if the maximum output will be the 5A load.

Through-hole aluminum electrolytic high-frequency capacitors were chosen for the input and output. The feedback capacitor is a small film or ceramic 220 pF.

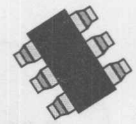
Tested data shows performance better than that of a PNP-based LDO, and the regulation is on par with standard NPN regulators (e.g. LM338). The dropout is very low for a 5A regulator, and line and load regulation is also very good.

Transient response is relatively quick, recovering within 60us from a 0-5A step.

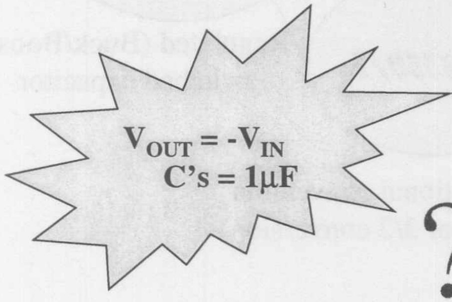
Why use a Switched Capacitor Converter?



NO INDUCTOR!
Saves cost, board space & height
Less radiated near field emissions



Ideal for low profile,
small board area designs



Easy to design, few equations
Minimum number of components

? Need a low-current voltage?
Don't want to use a complete switching regulator or linear regulator?
A switched capacitor may be your solution!

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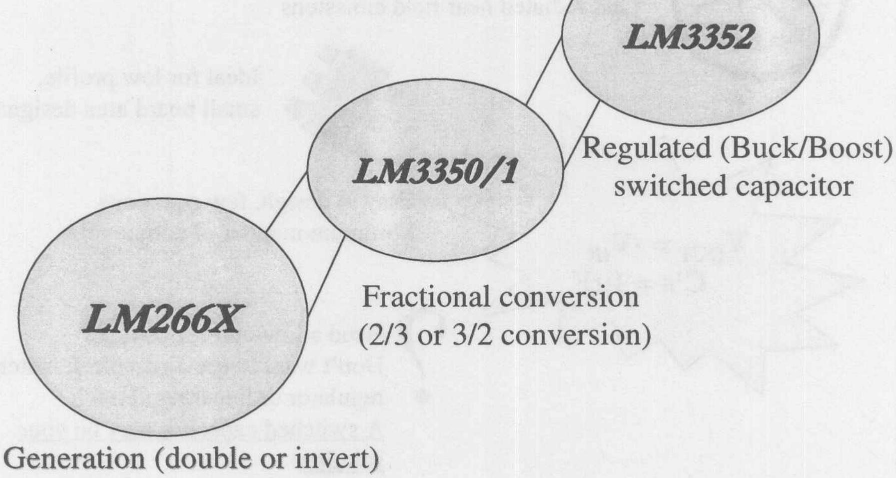
Switched capacitor converters can be an ideal solution in many low power applications. No inductor can mean cost and space savings over many inductive switchers. They come in small surface mount packages and require only a few small external capacitors so overall solution size can be minimized. They require almost no work to design with. You just add the capacitors and get the result you expect every time. It could also provide that extra little voltage your system needs. Have you ever found that you need a low current negative voltage to bias your op-amps? Use a switched capacitor converter! You don't need to design another whole inductive switcher into your system!

Innovations in Switched Capacitor Converter Technology



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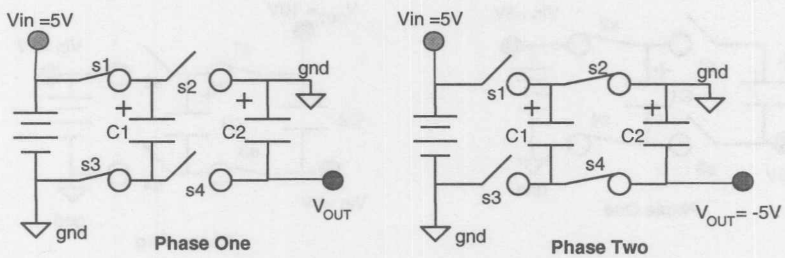
Switched Capacitor Converter Selection Guide

	Function	Package	I load	Efficiency	Sw.Freq.	SD Iq
First Generation						
LM2660/1	Dbl./Inv.	MSOP-8	100mA	88%	10/80kHz.	2uA
LM2662/3	Dbl./Inv.	SO-8	200mA	86%	20/160kHz.	10uA
LM2664	Invert	SOT23-6	40mA	91%	160kHz.	1uA
LM2665	Double	SOT23-6	40mA	90%	160kHz.	1uA
Innovation -- World's First Fractional Conversion						
LM3350	3/2 or 2/3	MSOP-8	50mA	90%	800kHz.	3uA
LM3351	3/2 or 2/3	MSOP-8	50mA	95%	200kHz.	3uA
New Products						
LM2682	**Double then invert (-2V_{IN})**					
LM3352	**Buck/Boost Regulator**					

The Basic Switched Capacitor Converter

Inverting Operation

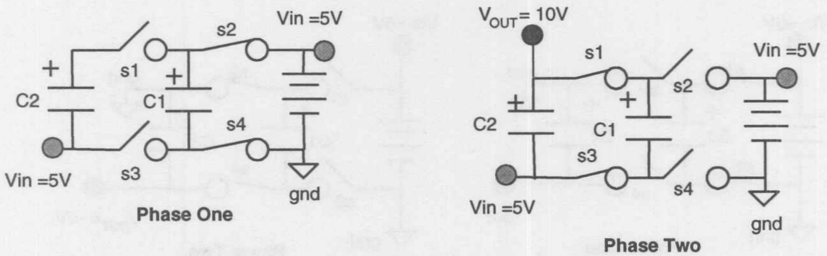


This shows how the basic switched capacitor function of inversion is achieved. In phase one switches 1 and 3 are closed and 2 and 4 are open. The input voltage charges the charge pump capacitor C1. In phase two switches 1 and 3 are open and 2 and 4 are closed. C1 transfers the energy to the output capacitor C2. The positive terminals of both capacitors are now tied to ground and the negative terminals have become the output. The result is a negative output voltage equal to the input voltage.

The Basic Switched Capacitor Converter

Doubling Operation (use it backwards!)

- Note: Input voltage (5V in this case) connected to two nodes.



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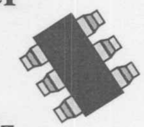
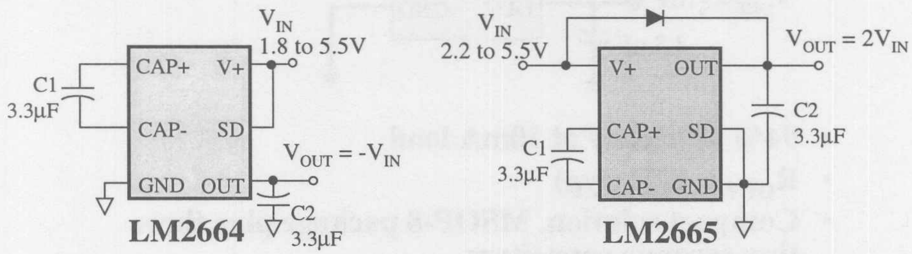
This shows how the basic switched capacitor function of doubling is achieved. In phase one switches 2 and 4 are closed and switches 1 and 3 are open. The charge pump capacitor C1 charges to the input voltage during this phase. In the next phase switches 1 and 3 are closed and 2 and 4 are open. C1 transfers its charge to the output capacitor C2. But notice that the input voltage is also applied to the negative terminal of C2 in this configuration. The capacitors that are charged to the input voltage are put in series with the input voltage so the net result is a positive output voltage the value of twice the input voltage.

LM2664 Inverter, LM2665 Doubler



- **Small package, small capacitors with 160kHz oscillator frequency**
- **Delivers 40mA load at 91% efficiency**
- **1µA shutdown supply current**



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The LM2664 switched-capacitor inverter can be used in an ultra-small converter solution because of its tiny SOT23-6 package and higher switching frequency. At 160 kHz, only two 3.3µF ceramic capacitors are needed to invert a 1.8 to 5.5V supply to a negative output, with typically 91% efficiency at a full 40 mA load.

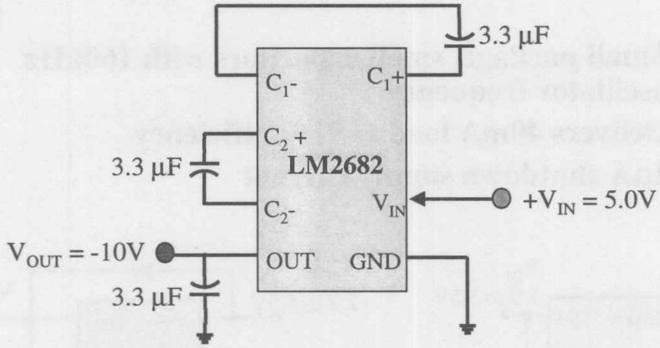
A shutdown control is available. When activated, the LM2664 turns off, drawing only 1µA (typ) from the source.

The LM2665 doubler is a complement to the LM2664 inverter. It is available in the same tiny SOT23-6 package, with similar specifications, but is customized for the different application. Because of its switch configuration, the LM2665 can also be run "backwards" to operate as a rail-splitter, dividing the input supply by 2.

The additional diode is a Schottky type, and is only used for start-up. The internal oscillator operates from the voltage between the OUT pin and the GND pin. This voltage must be greater than 1.8V to ensure operation of the oscillator. During start-up the diode is used to charge C2 to bring up the voltage at the OUT pin, allowing the oscillator to start.

In most cases, a 1A diode such as the 1N5817 is a good choice. If the input voltage ramp is less than 10V/ms, a smaller Schottky diode like the MBR0520LT1 can be used to reduce circuit size.

The LM2682 Doubles and Inverts!



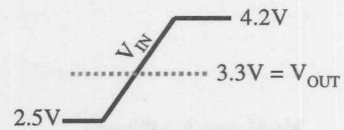
- **94% efficiency at 10mA load**
- **R_{OUT} = 10Ω (typ)**
- **Compact solution, MSOP-8 package plus three tiny ceramic capacitors**

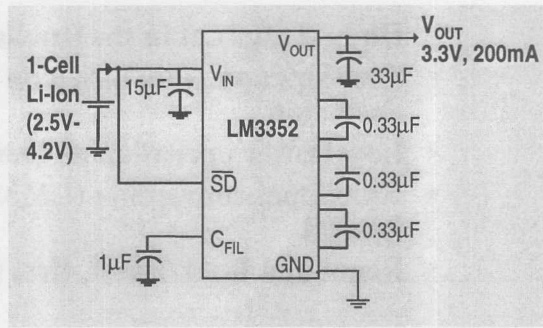
By arranging the configuration of switches and capacitors new functionality can be achieved as in this device, the LM2682. The device takes the input voltage and inverts and doubles it, so that the output voltage is -2x input voltage.

The LM2682 can deliver up to 10mA of output current with an efficiency of 94% (typical). The output impedance is 180Ω maximum at room temperature, typically 100Ω. The input voltage range is 2.0V to 5.5V, producing an output voltage of from -4V to -11V. This range is ideal for negative biasing when required for FETs. Specific applications include LCD bias, and GaAs power amplifier bias.

LM3352: True Buck-Boost Regulation!

- **2.0V to 5.5V Input**
- **Factory Set Output**
  - 2.5V, 3.0V, 3.3V…
  - 200mA Output
- **>80% Efficient Over Li-Ion Input Range**
- **1MHz switching frequency**
- **Regulates over line and load change conditions!**





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The LM3352 is a new power converter that is regulated without the use of a linear regulator or inductive switching regulator. The output voltage is digitally programmed at the factory for 2.5V, 3.0V, and 3.3V, but custom voltage options are available from 1.8V to 4.0V. Regulation is achieved by having a number of different gain stages. The output is digitally monitored and the IC automatically jumps to the correct gain depending on the input voltage and the load current. This circuit achieves an output tolerance of 4% over line and load conditions.

Delivering load current of up to 200mA, the LM3352 has variable output resistance depending on the ratio of input to output voltage. With a load of 50mA and a 33µF output capacitor, output ripple is typically 75mV. Operating quiescent current is less than 500µA (300µA typical), and in shutdown mode is reduced to typically 5µA.

Is your input voltage supply between 2.5V and 5.5V? Maybe a Li-Ion battery? Do you require step-up, step-down, or both? In this situation an LM3352 can save space, time, and money. The overall design time and solution size can be reduced over using an inductive switching regulator circuit, especially if an additional LDO would be required. With no inductors or diodes required, overall system cost can be reduced as well! The total solution, using the LM3352, requires only the IC in TSSOP-16 package, three tiny 0.33µF ceramic capacitors, a 1µF filter capacitor, and the input and output tantalum (Sprague type 592D) filter capacitors.

Why Use National Switched Capacitor Converters?

National offers:

- **Highest current in the smallest package**
- **Smaller capacitors based on higher frequency operation**
- **Low Power operation and shutdown**
- **Fractional conversion (LM3350/1), first in the market**
- **Regulated Buck/Boost, first in the market**

Look to National for the latest innovations in Switched Capacitor solutions for very convenient power supply enhancements.

Precision Voltage References

Reference Type	Product	Voltage	Initial Accuracy (%)
Bandgap	LM4040	2.5, 4.1, 5, 8.2, 10	0.1, 0.2, 0.5, 1.0, 2.0
	LM4041	1.2, Adj	0.1, 0.2, 0.5, 1.0, 2.0
	LM4431	2.5	2.0
	LM431	2.5/Adj	0.4, 0.8, 2.0
	LM113/313	1.2	1.0, 2.0, 5.0
	LM136/236/336-2.5	2.5	1.0, 2.0
	LM136/236/336-5.0	5	1.0, 2.0
	LM185/285/385-1.2	1.2	0.5, 1.0, 2.0, 3.0
	LM185/285/385-2.5	2.5	0.5, 1.0, 2.0, 3.0
	LM185/285/385	Adj	0.5, 1.0, 2.0, 3.0
Buried Zener	LM329	6.9	5 (Tempco as low as 10ppm/°C)
	LM199/399	6.9	2 (Tempco as low as 0.5ppm/°C)

- New Developments are Ongoing to Continually Improve on Critical Performance Specs (Tolerance, Noise, Drift and Operating Current) and Package Size
- Developments are Re-Applied to Other Products such as Lithium Ion Battery Chargers!

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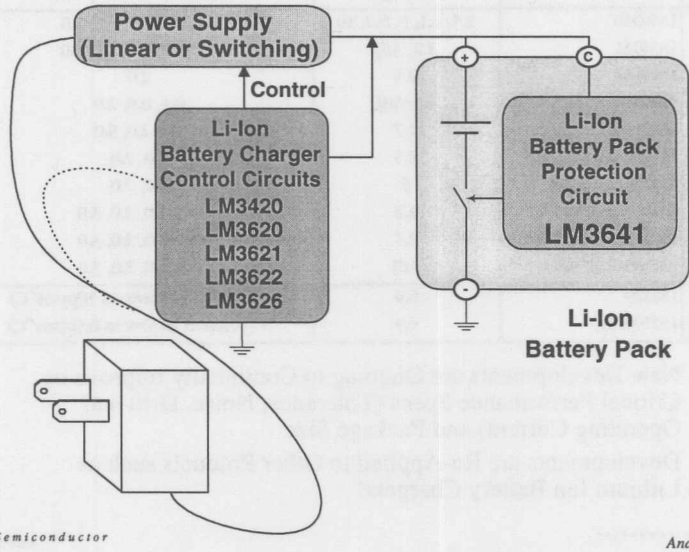
Analog Solutions 49

Voltage References are still a very important product development area at National.We continue to develop devices with tighter tolerances and reduced drift, noise and operating currents.

As developments are made, the technology used for precision references gets re-applied in other product developments. Here is a family of devices used to precisely control the charging and voltage of Lithium-Ion battery cells. Each circuit is made possible by using a precision Voltage Reference.

Lithium-Ion Battery
Charge Control and Protection Circuits



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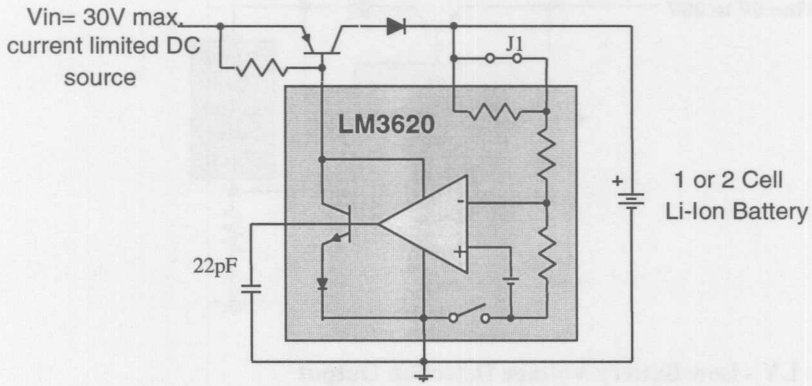
Lithium-Ion batteries offer much greater energy density, in terms of both weight and battery life, compared to Ni-Cd of Ni-Mh batteries. However, they require more support circuitry to assure their long life and safe use.

Accuracy in charging a Li-Ion battery is of paramount importance because for every 2.5% error in voltage detection accuracy, there would be a 15% reduction in pack capacity.

Additionally, protection must be provided against accidental misuse such as over discharge or excessive current withdrawal to preserve the battery packs life cycle and its safety.

We will be discussing solutions for battery protection as well as charging during this part of the presentation.

Multi-Anode, Multi-Cell Li-Ion Charger



J1 Short for Graphite Anode (4.1V/Cell)
Open for Coke Anode (4.2V/Cell)

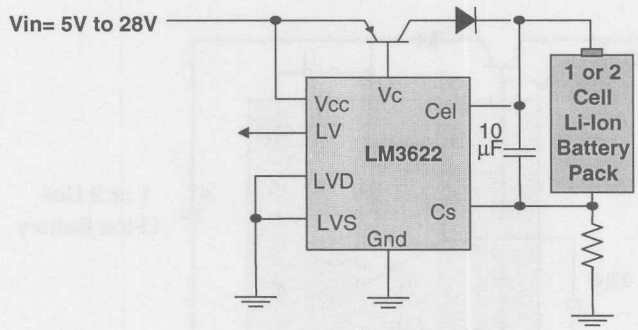
This very simple and small linear charger is configurable for charging Li-Ion batteries with Coke or Graphite Anodes.

The constant voltage charge controller, LM3620, has options to charge 1 or 2 cell stacks with better than 1.2% voltage accuracy.

Charge current is limited to the current provided by the input supply and the external pass transistor.

The internal power off detector disconnects the charger from battery when input supply is disconnected limiting the leakage current to less than 10nA.

Simple Li-Ion Battery Charge Controller With Low Battery Detector Output



- **LV - Low Battery Voltage Detection Output**
- **LVS - Low Battery Voltage Threshold (L=2.70V, H=2.15V)**
- **LVD - Low Voltage Detection Disable (LVD = H, enable LVD = L)**

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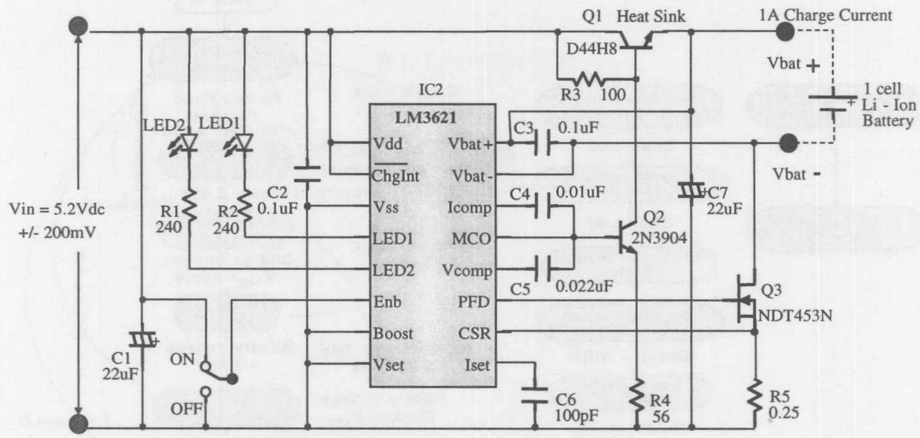
When a basic lithium-ion charge is needed, the LM3622 charge controller can be used with a few external components to make a very simple solution. This basic charger circuit also contains low battery voltage detection circuitry.

The open collector output of the low battery detector circuit is pulled low when the battery voltage is below a preset selectable level.

The threshold level is set to 2.7V in this circuit but it can be set to 2.15V by pulling the LVS pin to Vcc.

The charge control pin, Vc, sinks current when battery voltage is below the regulation. Voltage at the Cs pin controls the charge current.

1 Amp Li-Ion Charger Controller



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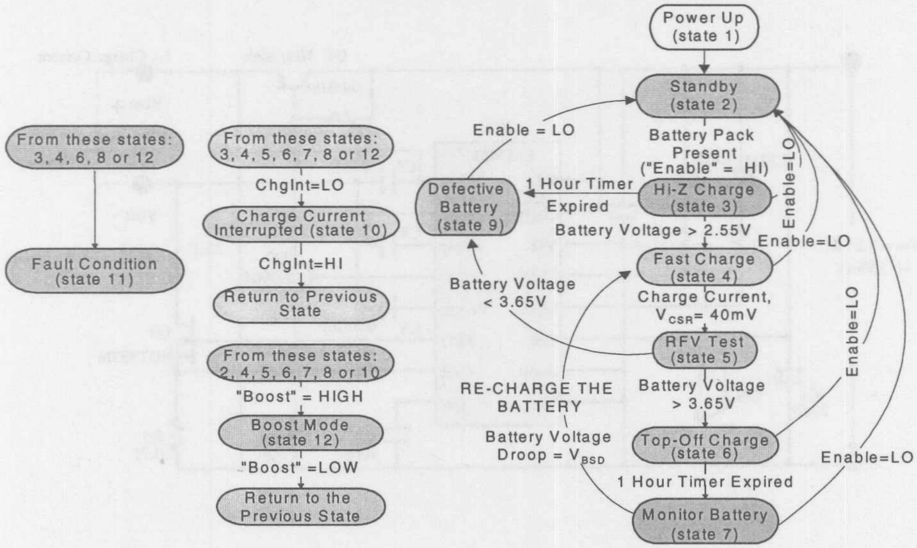
Analog Solutions 53

For a full-featured Constant Voltage, Constant Current (CVCC) lithium-ion battery charger, the LM3621 can be used. The LM3621 controls all phases of the charge from conditioning, fast charge, top-off, monitor and maintenance. Status of charge is displayed by the two LEDs.

The circuit is configured for charging batteries with a Graphite (4.1V) anode, but it can be easily configured to charge batteries with a Coke (4.2V) anode by simply pulling the V_{SET} pin high. R5 sets the maximum fast charge current.

LM3621 Charge State Diagram



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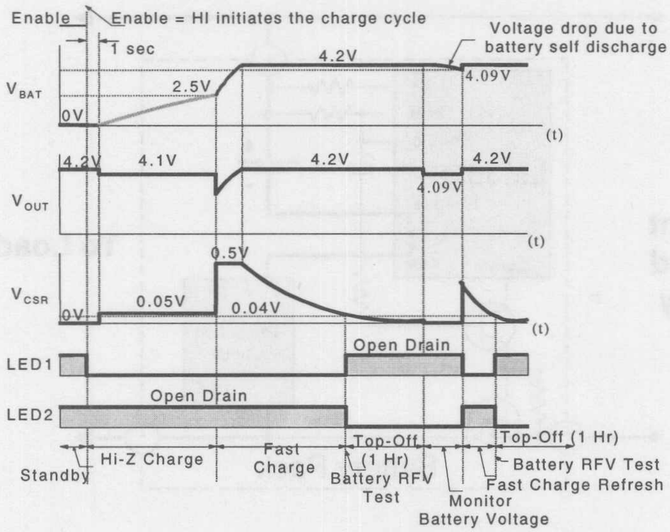
A Finite State Machine logic controller is built into the LM3621. This state diagram illustrates the full capabilities of this complete battery charge controller. While the state diagram may appear very complicated, it serves to automate the complete charge cycle and makes it easy to configure and use an LM3621-based charger.

LM3621 Charge Cycle Waveform



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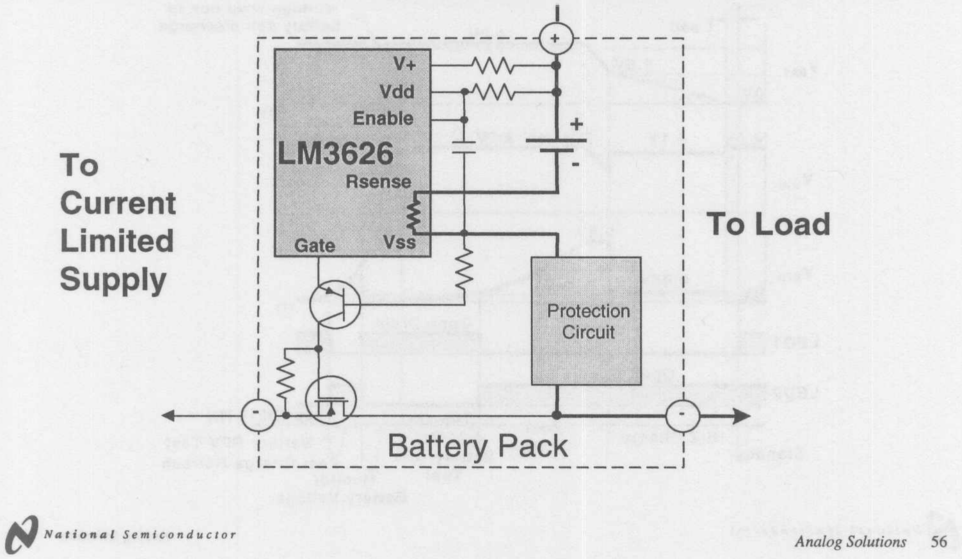
Analog Solutions 55

A typical charge cycle illustrates all the control modes of the LM3621.

The green V_{BATT} trace (from 0V to 2.5V) indicates the battery voltage during preconditioning. The red trace, from 2.5V to 4.2V, represents the LM3621 fast charge operation in Constant Current mode. The blue trace, from 4.2V until self-discharge begins, indicates the transition to Constant Voltage mode.

Transition to Top-Off mode is indicated by the LED1 turning off and LED2 turning on.

During the maintenance mode, the LM3621 monitors the state of charge in the battery. LED1 turns on and LED2 will turn off for brief periods of time when the cell is topped-off.

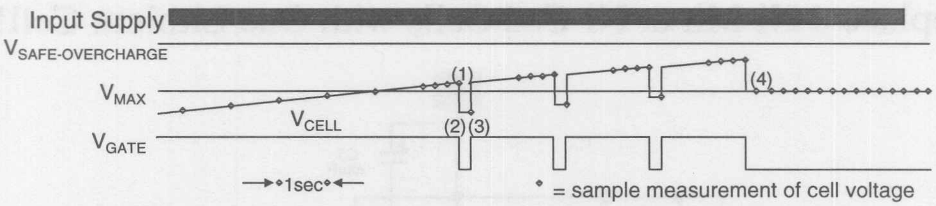


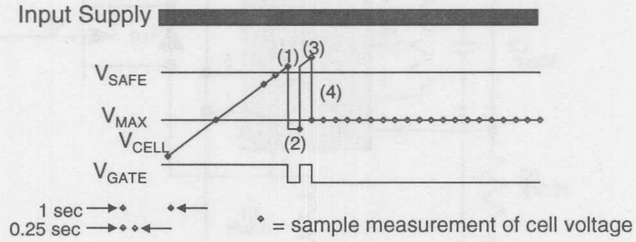
This current pulse charger is designed to reside inside the battery pack to take advantage of the higher battery voltage monitoring accuracy achieved by eliminating the errors caused by the contact resistance of the external connectors.

LM3626 monitors the battery voltage with better than +/-25 mV accuracy. It also limits the charge current, which is monitored by measuring the voltage across an internal 4mΩ resistor. The maximum charge current is factory programmed between 1A and 4A with 0.5A accuracy.

The details of the Li-Ion protection circuit IC are presented on the next page.

In-Pack Charger Timing Diagram





The charge control function of the LM3626 is illustrated in this timing diagram.

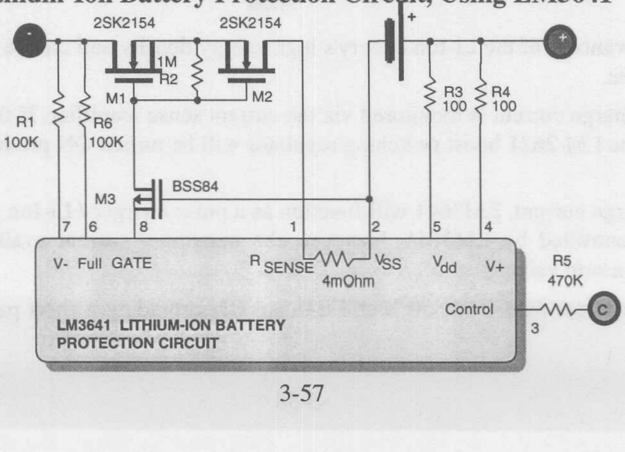
For battery voltages below Vbatt, the MOSFET switches are ON and the maximum current available from the source (Icharge<Imax) will charge the battery. The battery voltage is sampled every second and compared to Vbatt limit set internally in LM3626.

If a battery voltage higher than Vbatt but less than Vsafe is detected, the sample rate is increased to 4 samples a second. After detecting 4 consecutive samples of >Vbatt, the MOSFETS are turned OFF disconnecting the charge current to the battery.

If battery voltage exceeds Vsafe, Charge is terminated immediately.

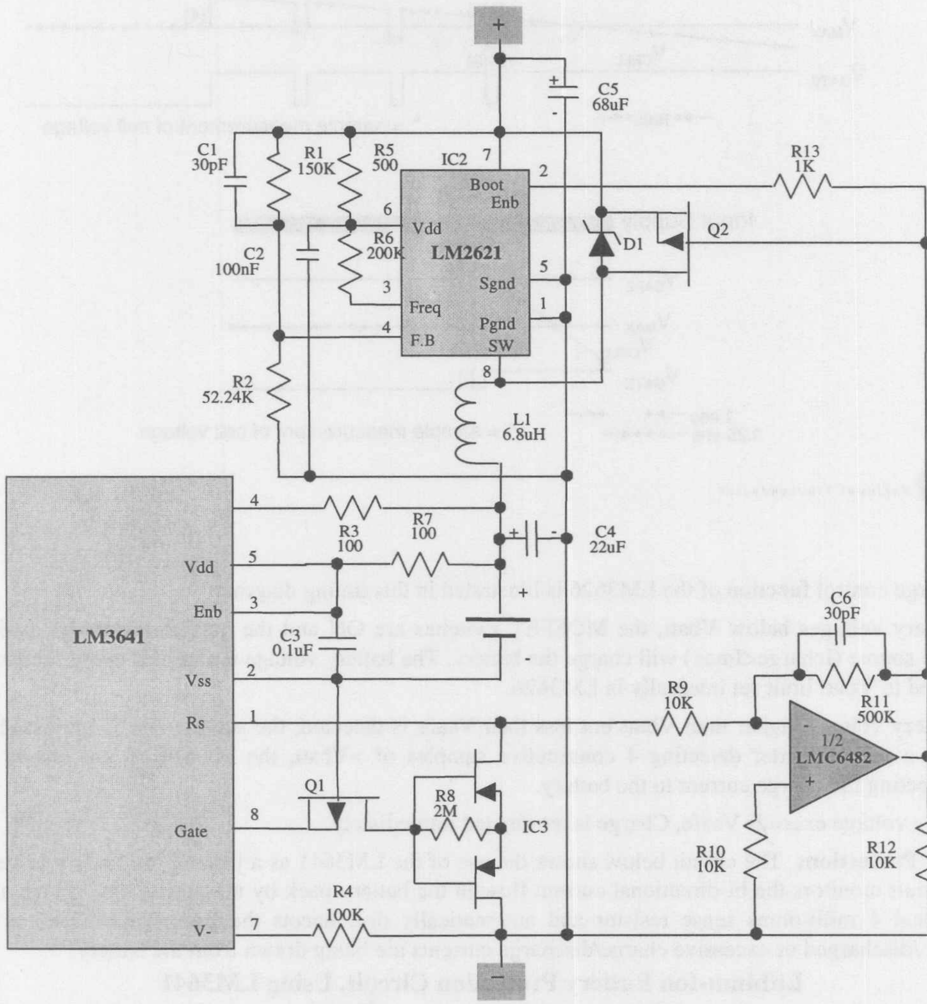
Battery Protection: The circuit below shows the use of the LM3641 as a lithium-ion battery protector. This circuit monitors the bi-directional current flow in the battery pack by measuring the voltage across an internal 4 milli-ohms sense resistor and automatically disconnects the battery when cell is over charged /discharged or excessive charge/discharge currents are being drawn from the battery.

Lithium-Ion Battery Protection Circuit, Using LM3641



4.8V Li-Ion Battery

(Replace 4 Ni-Mh or Ni-Cad Cells with One Lithium Cell!)



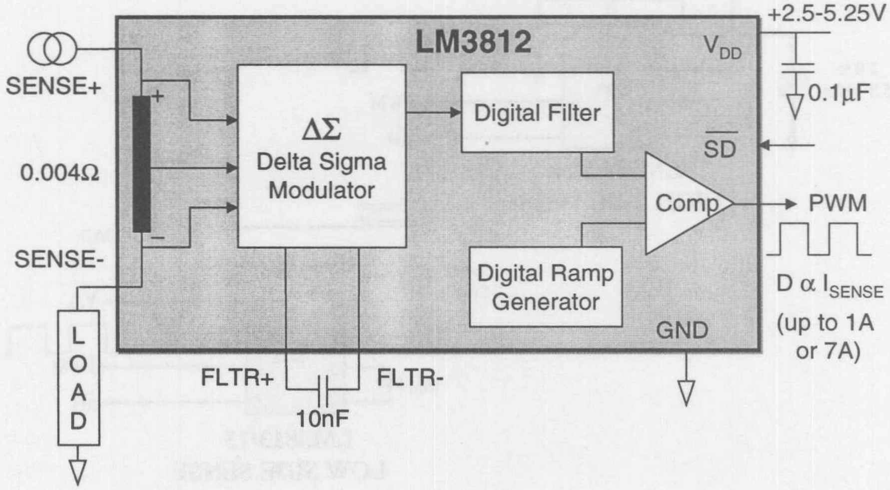
This circuit takes advantage of the Li-Ion battery's high energy density and charge cycle to replace 4 Ni-Mh or Ni-Cd batteries.

The charge and discharge current is monitored via the current sense amplifier. If the discharge current is greater than 1 uA, the LM 2621 boost switching regulator will be turned ON producing 4.8V across the pack terminal.

If circuit detects charge current, LM3641 will function as a pulse charger / Li-Ion protection circuit. The charge current is controlled by LM3641, however, the maximum current available from the source should be limited to a safe value.

For discharge currents less than 1 uA, all MOSFETs are ON providing a short path from the battery to the pack terminals.

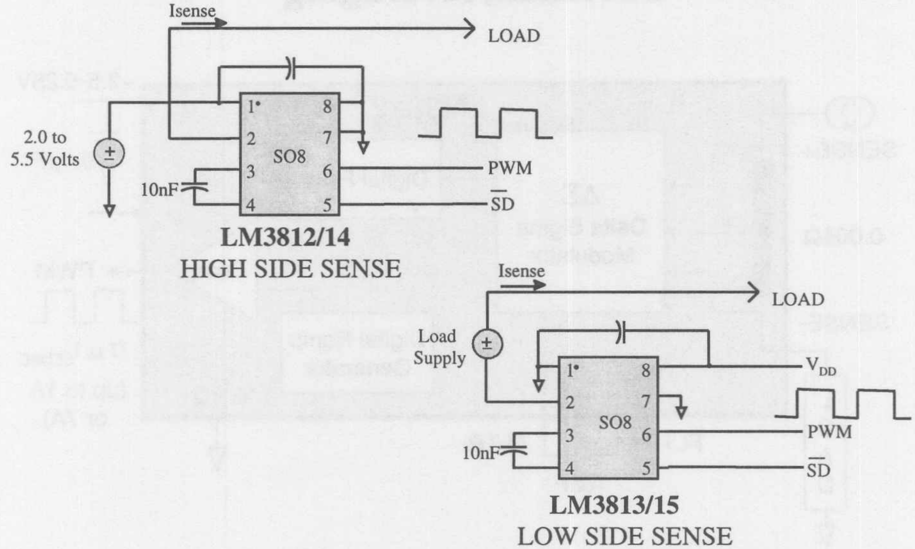
Current Sense Uses ΔΣ A/D Converter for Precision, Averaging



While a simple resistor can be adequate for sensing current, getting high precision for high current levels (1-10A) in a production environment can be expensive. In addition, the resulting voltage usually needs to be filtered and converted from analog to digital before use by any digital monitoring system.

An alternative approach, used in the LM3812/13/14/15, uses a precision-trimmed 4mΩ leadframe resistor with integrated delta-sigma analog-to-digital converter, digital filter, and pulse-width modulated output converter. If desired, the PWM output can be directly applied to a microcontroller input to monitor the average current level. Two sense current ranges are available, 1A and 7A (10A peak).

LM3812/13/14/15 Current Gauge ICs



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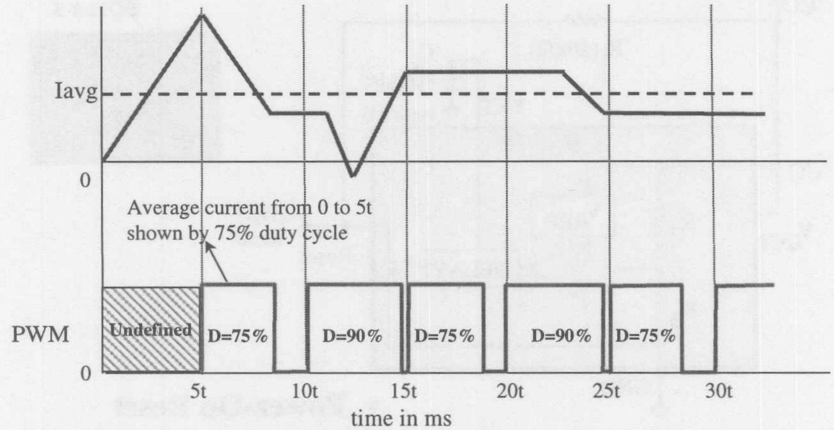
Eight variations of the LM381x family are available. Two part numbers, LM3812 and LM3814, are for low-side sensing, while the LM3813 and LM3815 are for high-sensing. (Low-side is sensing current near ground, while high-side is sensing current near V_{DD}.)

Two different sample times are available, 6 ms (fast mode- LM3814 and LM3815) and 50 ms (precision mode- LM3812 and LM3813). This denotes the period of time over which the current is averaged. The average accuracy's of both sample times are approximately the same; the fast mode offers faster readings but with a little more jitter.

The sense current ranges are 1A and 7A. The 1A parts read 1A full scale (95.5% or 4.5% duty cycle), while the 7A parts read 10A full scale. 10A operation is rated for no more than 200 ms.

	High-Side	Low-Side
Precision (50 ms sampling interval)	LM3812	LM3813
Fast (6ms sampling interval)	LM3814	LM3815

LM381x Duty Cycle Proportional to Average Current During Sample Period



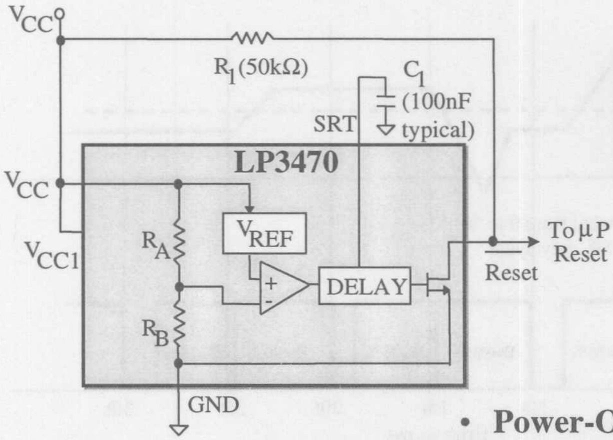
t = 1.2 for LM3814/15
t = 10 for LM3812/13

As shown above, duty cycle of the PWM waveform during any sampling interval indicates the current magnitude (average) and direction during the previous sampling interval. The sampling time is 6ms for LM3814/15 and 50ms for LM3812/13. The IC can sense currents from -Imax to +Imax. Options for Imax are 1A (LM3812, LM3814) or 7A (LM3813, LM3815). From the duty cycle, the sensed current can be calculated using the formula:

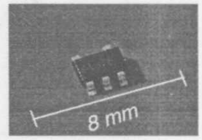
$$Isense = 2.2(D-0.5)Imax$$

While this formula can be used to translate between current level and duty cycle, the product datasheets also contain conversion tables for duty cycle to current, and current to duty cycle.

LP3470 Voltage Supervisor



Integrated TinyPak
SOT23-5



- **Power-On Reset**
- **Threshold Detect**

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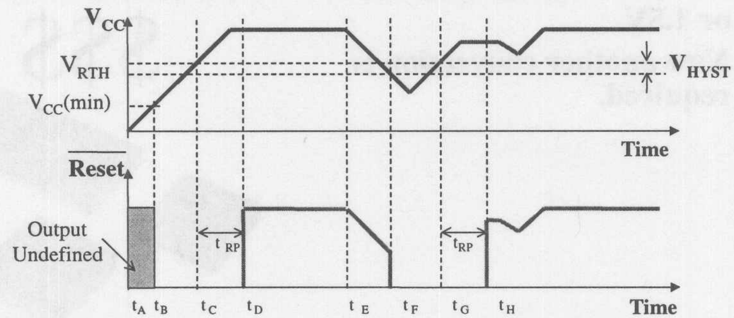
Integrating the functions of a precision reference, a comparator, and a one-shot timer, the LP3740 is a micropower CMOS voltage supervisor designed to monitor power supplies in microprocessor/microcontroller and similar digital systems. With the ability to monitor the applied supply voltage at the point of load, the LP3470 is ideal for distributed supply systems. It is equally at home in battery-powered equipment as in line-powered systems.

The LP3740 produces a reset signal ("flag") whenever the V_{CC} supply voltage falls below the reset threshold. When the supply voltage recovers, the flag remains asserted for a reset time-out period. An external capacitor determines the length of the reset time-out.

With no external capacitor to set a reset time-out, the LP3740 functions as a threshold detect. It will produce a flag only during the time that V_{CC} is below the reset threshold. When V_{CC} rises above the threshold (plus the built-in hysteresis of typically 35 mV), the flag is released.

Adjustable Reset Delay

- **External capacitor sets delay**
  - 100 µs is minimum delay; max. based on capacitor leakage
  - t_{RP} (ms) = 2000 x C_1 (µF); this is 100x longer per µF than competition
  - Typical delay range 50ms to 200ms (25nF to 0.1µF)
- **Rejects short transients**



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Analog Solutions 63

The reset time-out period is set with an external capacitor connected between pin SRT and ground. The capacitor value is determined by the time-out period desired:

$$t_{RP} \text{ (ms)} = 2000 \times C1 \text{ (uF)}$$

With no external capacitor, the intrinsic delay of the LP3740 is about 100 us, assuming that V_{CC} is falling or rising at 1mV/us. The practical range of the reset delay is limited primarily by capacitor leakage.

A small amount of hysteresis has been added to the LP3740 to prevent the flag from "chattering" when V_{CC} is near the threshold. Once V_{CC} has crossed the threshold and set the flag, the flag will remain at its set value until V_{CC} exceeds the threshold in the opposite direction by more than the hysteresis, typically 35mV.

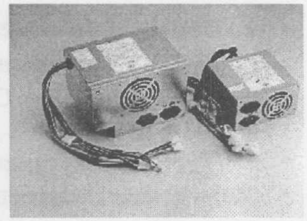
To improve noise rejection, the LP3740 is relatively immune to short negative-going V_{CC} transients. A 0.1uF bypass capacitor mounted close to the V_{CC} pin provides additional transient immunity.

At low input voltages, below 0.5V, the reset flag is not valid.

Low Voltage Conversion

- **5V rails are common and inexpensive.**

  BUT
- **New digital ICs run at 3.3V, or 2.8, or 2.5, or 1.8, or 1.5V**
- **Now another conversion is required.**



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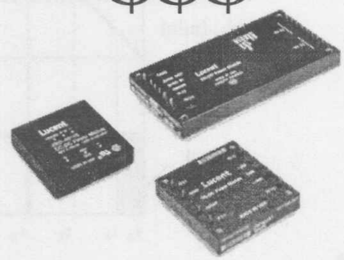

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Analog Solutions 64

Many systems today use a significant amount of 5V power. AT power supplies and other AC/DC converters provide regulated 5V from the wall. DC/DC bricks provide 5V in telecom applications. Many linear supplies are available to provide 5V at lower power.

You just decided to upgrade your existing platform and the latest and greatest digital ICs are rated at 3.3V or less. Where will you get the 3.3V???

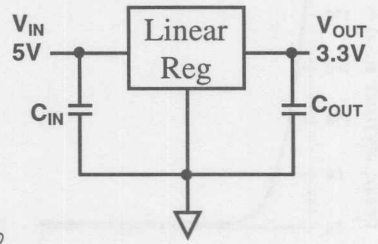
You could buy a second module, but that will tend to be costly. Multiple output DC/DCs are availble, again at a price premium. You could buy an ATX supply with 3.3V available (but if your IC requires 2.5 or 1.8 you still have a problem).

Probably one of the best ways to get your lower output voltage is to use a National Seminconductor linear or switching regulator running from your existing 5V supply. The supply can be sized for exactly what you need, and the proven solutions are much more cost effective than an off-the-shelf module.

In the following section we will also look at solutions which can convert 5V to those lower voltages you need, or 3.3V to those lower voltages.

Low Current and Low Cost?
Let's use a linear regulator

5V(±5%) - 3.3V(±1%) = 1.41V dropout required
5V(±5%) - 3.3V(±5%) = 1.28V dropout required



Typical Efficiency is 66%
In many application this is OK,
but look out for the HEAT

The simplest and cheapest way to step 5V down to 3.3V is to use a linear regulator. However, you need to make sure that the dropout voltage of the linear is lower than the minimum voltage differential in your application. NPN regulators have about 2V of dropout, so they are not appropriate for this application. LDOs and quasi-LDOs are the best choice. *Refer to page 29 for the differences between regulator types.* National has a lot of products that meet the needs of this application (check out a selector guide). The newest products are:

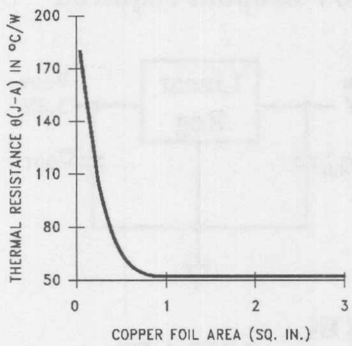
LP3480/90	100mA (quasi-LDO)
LP2966	2x150mA (CMOS LDO)
LP2986/7/8	200mA
LM1117	800mA (quasi-LDO)
LP2975	P-FET Controller (about 5Amps practical)

Now lets consider the down side to using a linear - power loss, power dissipation, and heat. Nothing we can do about it, 3.3/5 = 66% efficiency. Now add in ground pin current (Iq) and it gets worse. Worst case Efficiency = 100*(Voutmin*Iout)/(Vinmax*Iout+Vinmax*Iq). And lower efficiency means higher power dissipation! Also, compare ground pin currents when doing your design. The LM1117 is a quasi-LDO and has much less Iq than an old LM3940, 100uA@800mA out vs 100mA@800mA out!! The LP298X series uses a super-beta process and has about 1-2mA Iq for a 200mA output current. The LP2966 is a CMOS part and has 400uA Iq for 200mA The best case is the LP2975 where 5Amps of current on the output only results in 180uA of ground pin current. Make sure to pay attention to your thermal design. 125C is the maximum die temperature for our devices. Small packages are nice, but they don't get rid of the heat!

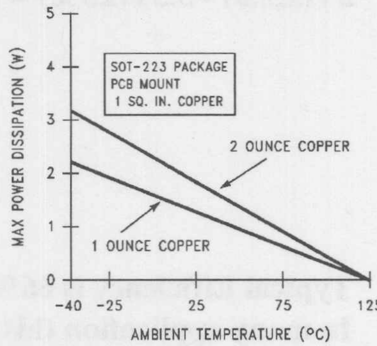
When converting 3.3V to 2.8V or 2.5V and 2.5V to 1.8V, the voltage differential is less. As a result, power dissipation is less and a linear regulator becomes even more practical. The LP2966, LP295X, and LP298X series of LDOs can support these low voltage conversions.

SOT-223 Thermal Considerations

$\theta_{(JA)}$ vs Copper (2 ounce) Area for the SOT-223 Package



Maximum Power Dissipation vs Ambient Temperature



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Analog Solutions 66

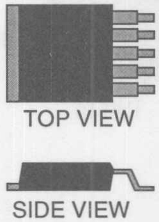
Surface-Mount Power with SOT-223 "MP" Package

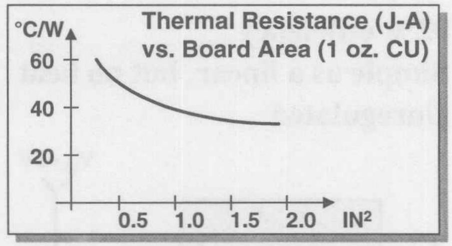
The SOT-223 ("MP") package uses a copper plane on the PCB and the PCB itself as a heatsink. To optimize the heat sinking ability of the plane and PCB, solder the tab of the package to the plane.

As shown in the left figure, increasing the copper area beyond 1 square inch produces very little improvement in thermal resistance. The figure on the right shows the maximum allowable power dissipation compared to ambient temperature for the SOT-223 device (assuming θ_{JA} is 74°C/W for 1 ounce copper and 51°C/W for 2 ounce copper and a maximum junction temperature of 125°C). These curves show the effects of adding copper on the back side of the PCB (with no solder mask over the copper). A further reduction of 10 to 15°C/W can be achieved if the copper area is on the component-side of the PCB.

These curves were excerpted from the LM2940 datasheet, but apply as well to the LM1117, LM317, LM337, LM340, LM2937, and LM3940 regulators in the SOT-223 package.

Surface-Mount Power With TO-263 “S” Package





- **Board area of TO-263 is 0.136 in^2**
- **Minimum θ_{J-A} is 32 °C/W**
- **OK for standard surface mount soldering**

National Semiconductor *Analog Solutions* 67

Surface-Mount Power with TO-263 “S” Package

National Semiconductor also has the surface-mount power package, TO-263, registered by JEDEC. Resembling a TO-220 type package with the tab cropped and leads in gull-wing bend, the TO-263 can be soldered to a p.c. board using standard vapor phase or infrared techniques (260°C max. at 10 sec.). Because the IR soldering temperature is higher than that used for TO-220 devices, a special high lead solder material is used for the die attach in the TO-263 packages.

Products in both the 3-lead, 5-lead, and 7-lead version of this package are now available. The part number designation for this package is an “S” suffix.

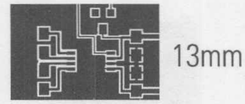
While the TO-220 package often depends on a the use of metal heat sink to reduce the package thermal resistance, the TO-263 must depend on the use of copper in the p.c. board. With only 1 square inch of copper thermally connected to the package, the thermal resistance (junction to ambient) is reduced to 37 °C/W (typ.). Additional copper area will reduce the thermal resistance further, to a minimum of 32 °C/W at over 1.6 in2.

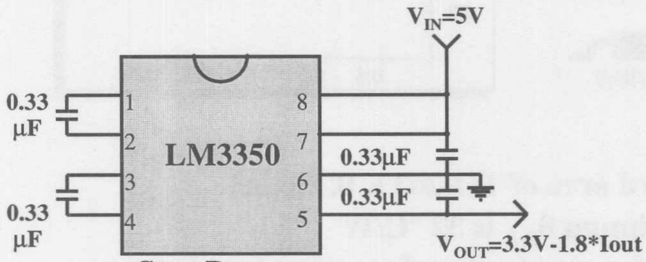
A wide variety of devices are available in this package. From LDOs, like the LP2956, to the latest Simple Switcher, the LM2679.

50mA Fractional Converter LM3350

- **92% efficiency**
- **Simple as a linear, but no heat**
- **Unregulated**

Board Layout





Step Down Converter

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Analog Solutions 68

The LM3350 is a fractional charge pump converter. It steps down by a ratio of 2/3 to take 5V and give 3.3V or 3.3V and give 2.2V. Typical conversion efficiency is 92% at a 50mA load. Beats a linear. You also don't need to worry about output capacitor selection for stability.

In the step-down mode, only 4 - 0805 size 0.33uF capacitors, are required. Combined with the Mini SO-8 package, the size of the complete function is minimal.

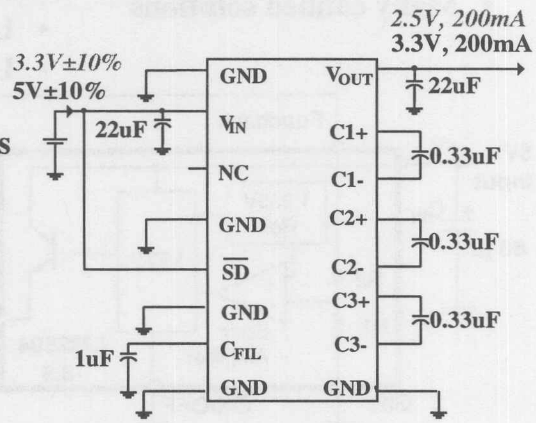
Like most switched capacitors, the output is not regulated. However, there will not be much variation with load with its output impedance of only 1.8ohms. This means: $V_{OUT} = V_{IN}$ x0.667- I_{OUT} x1.8. So make sure to consider input voltage tolerances in your calculation. Also look at the input operating voltage range for the devices you will be powering. In many cases, operating voltages are 3.0 to 3.6V.

In step-down mode, activating the shutdown reduces the quiescent current to 1uA. That makes this part an ideal selection for battery powered applications.

Another way to use the part is to provide a reduced input voltage to a linear regulator. This way you get high efficiency and a regulated output. For example, 3.3Vin to 2.2V to 1.8V after the linear. This way, efficiency goes from 54% to 82%. In an application powered from the wall, we probably don't care about the efficiency because the heat from 160mW of loss is trivial. In battery powered systems, battery life is the name of the game, and every little bit helps.

LM3352: Regulated Switched Capacitor

- True Regulated Switched Capacitor
- 85% efficiency
- 200mA Output
- TSSOP-16
- All ceramic caps



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You have seen this part earlier in the presentation. The LM3352 provides a true regulated output voltage without post regulating with a linear. This is truly a "cool" part. It can convert 5V to 3.3V and 3.3V to 2.5V both at 200mA! Conversion efficiency is very good with a typical of 85%.

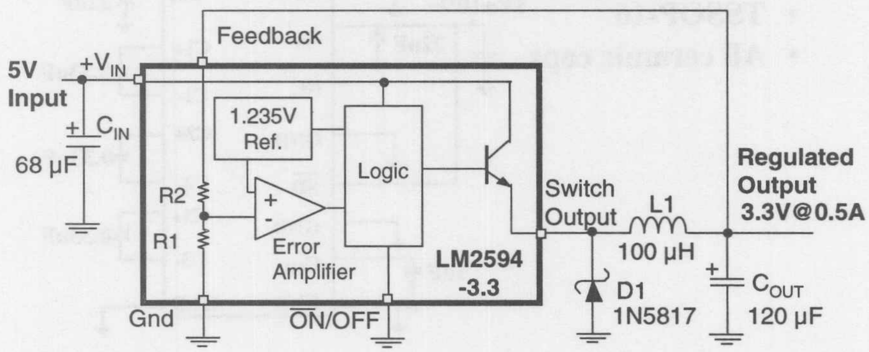
The internal digital control means no worrying about stability.

For output and input capacitors, check out Taiyo Yuden part number LMK432BJ226. These will give you the lowest input and output ripple in your application.

Switching Buck Regulators

- Provide the best efficiency, up to 95%
- Many canned solutions

- Simple Switchers
- LM2630
- LM2635/6
- LM2650
- LM2651/3



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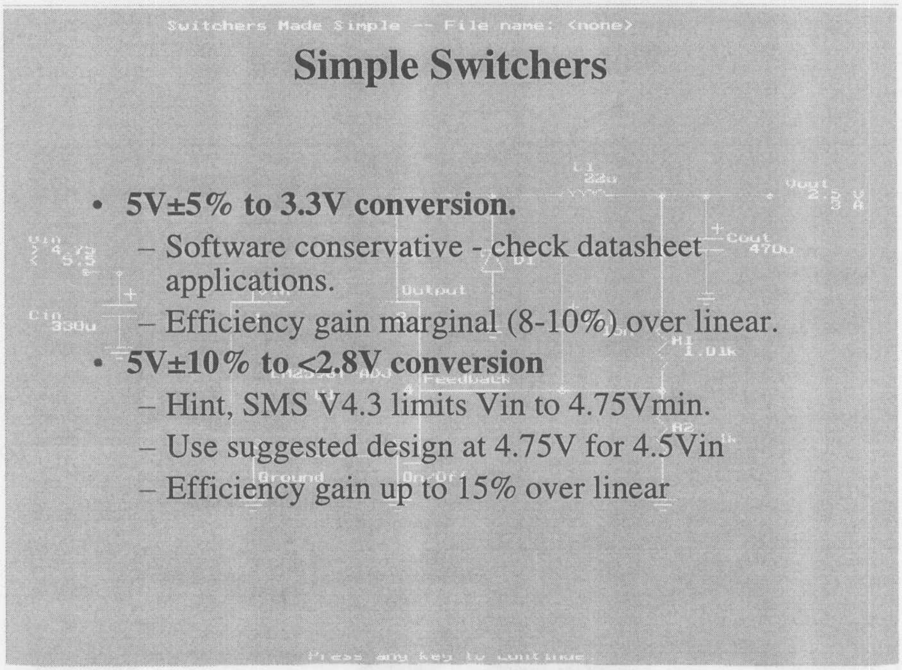
Analog Solutions 70

A step-down (buck) switching regulator is the most efficient way to convert a voltage to a lower voltage. If all the components were ideal, efficiency would be 100%.

The buck regulator works by simply creating a square wave voltage at the switch output and then LC filtering to get a DC output voltage. The average value of the square wave at the switch is the output voltage. If you go back to your EE and math books, you will find that Vave = D*V. In the case of a switching regulator, Vave=Vout, and V=Vin. The control loop controls "D", the time the switch is on, so the output voltage is controlled. This is the only switching topology that works in this manner. All others rely on the storage of energy in the inductor when the switch is closed and then release the energy to the output when the switch is open.



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Analog Solutions 71

The Simple Switchers (LM2594/5/6/7/8/9) will provide step down conversion from 5V. There are some things to pay attention too when using these devices for 5V conversion

These Simple switchers use bipolar switches. As a result, the voltage drop across the switch is 1V. At these low voltages, this switch voltage translates into poor efficiency compared to ***other*** switching regulators (don't panic - we sell the ***other*** regulators).

Now the best way to design with Simple Switchers is to use the Switchers Made Simple software. And for 3.3V outputs up to 1.5Amps out and 2.5V outputs up to 3.0Amps, no problem. However, at the highest current levels and low output voltages, efficiency may be only marginally better than a linear.

If you design for 4.75 - 5.25Vin and 3.3V @ 3Amp out the software says "5.29V minimum input voltage required". The software makes assumptions about input capacitor ESR, inductor DCR, and diode voltage and calculates switch saturation voltage. These assumptions work in most cases. When trying to get 3.3V from 4.75V one needs to move beyond the assumptions set in the program.

To get 3.3V from 5V at 3Amps using a LM2596 you need:

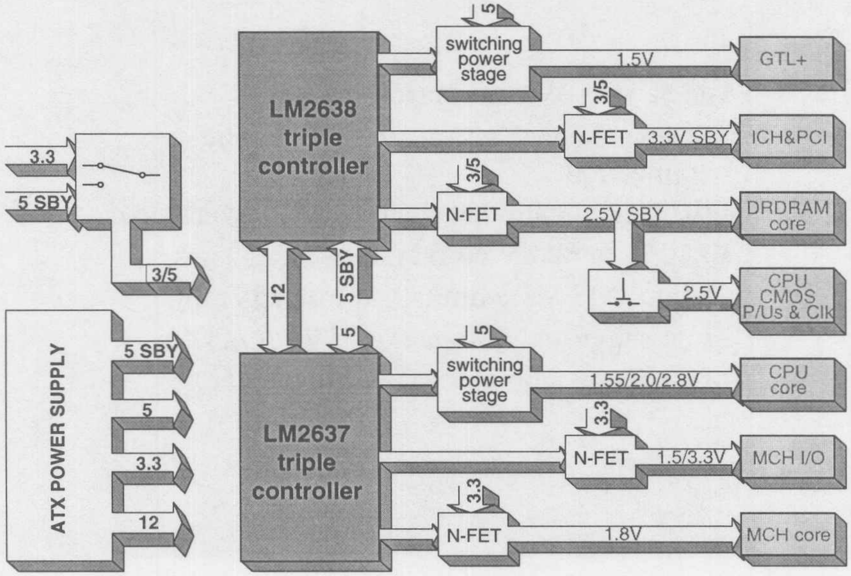
An input cap with extremely low ESR (44mohm for the cap on the datasheet)

An inductor with very little DCR (40mohm for the inductor in the datasheet)

An oversized diode (the datasheet uses a 5Amp diode)

Now for more of those ***other*** regulators.

Slot 1/Camino Solution



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Analog Solutions 72

Low voltage conversion can take on different levels of complexity. As an introduction to solutions using products developed for desktop Intel processors, the block diagram above shows a solution for the Intel Camino platform. Hopefully, your systems will not require this many voltages.

The Camino platform demands quite a few different voltages that need to be generated locally on the motherboard. Some of them are of the same voltage level but need to be power-managed separately. The slide shows seven different voltages for seven different loads. An LM2637 and an LM2638 combined can supply all those voltages. The CPU core needs a dedicated power supply due to its voltage's programmability and ultra fast load transient. The CPU core power supply can be controlled by the switching section of LM2637. It provides all the necessary functions such as power good, output enable, over-current protection and over-voltage protection. The GTL+ bus needs 1.5V, with a maximum load current of 4 to 6 amps. This makes a switching solution attractive and the switching section of an LM2638 can provide the control. The rest of the voltages have relatively low current and can be supplied through linear regulators. The standby voltages, such as the 3.3V SBY for the ICH (I/O Control Hub) and PCI, are voltages that are available whenever the PC's power cable is connected to the wall outlet. They are used to support STR (Suspend to RAM) or S3 mode. During STR, all the non-standby voltages are shut off. A dual voltage (3/5), generated with a FET switch, is used as the input voltage of the standby converters so that during full operation mode there is enough input power and during standby mode, there is input voltage. LM2638 is capable of controlling the two standby voltages (3.3VSBY and 2.5VSBY) because it has a charge pump pin and can generate a 10V off the 5V SBY during STR. This 10V voltage makes it possible to control the external N-FETs and regulate the standby voltages. The MCH I/O requires either a 1.5V or a 3.3V, depends on the graphics daughter card plugged onto the motherboard. The solution relies on a signal sent by the daughter card to determine whether the output is 1.5V or 3.3V.

The total solution is a quite cost-effective one. There is no need to use an external voltage doubler IC to generate the 10V during STR, and both IC's are fully utilized.

- **LM2635 and LM2636 are Pentium II VRM Controllers.**
  - 5V to 3.3V at 3Amps, Fs = 600kHz
  - 5V to 3.3V at 3Amps, Fs = 300kHz
  - 5V to 3.3V at 8Amps, Fs = 600kHz
    - » Vout is digitally adjustable!
  - Pentium II Power Supply
- **The LM2636 is preferred over LM2635 for new designs**
- **LM2637 and LM2638 add two LDO controllers to the switching regulator core.**

For higher output currents, the LM2635 and LM2636 are the parts to use.

The LM2635/6 is a 5-bit programmable, synchronous buck regulator controller. It was designed primarily for Pentium II desktop power supply requirements. The output voltage is programmable from 1.3V to 3.5V via the VID pins. So any of these designs on the following pages can be changed anywhere in that range by changing which VID pins are grounded. Input voltage of the buck regulators can be anywhere from 5V to 12V for the LM2636, but the LM2635 requires the 5V rail for the power Vin. PWM frequency is programmable from 50kHz to 1MHz, so you can use smaller inductors. Control scheme is voltage mode control.

PWM frequency is set by R2. Over-current limit is set by R3 minimum. The external MOSFET gate drives are powered from an external 12V source. If the 12V source is not available, it is also possible to generate it from 5V using a simple external charge pump (bootstrap circuit). The output voltage is programmed by the grounding pattern of the VID pins. This LM2635/6 is capable of providing output currents in excess of 15Amps. Low ESR output capacitors are required for a reasonable ripple voltage and good load transient response. Typically SANYO 10MV1200AX caps (5 to 8 of them, ESR < 44mΩ each) are used. The initial output voltage tolerance is 1.5% over a temperature range of 0 to 70 degrees Celsius. Other features are a power good flag, an output enable pin, and over-voltage protection. Whenever there is an over voltage at the output, the high-side FET will be turned off and the low-side FET be turned on immediately.

There is a VREF pin which supplies a buffered bandgap output (1.255V nominal) for use with other regulators. For example, four cheap linear regulators can be generated by using this VREF signal, an LM324 quad op-amp, and four N-channel MOSFETs.

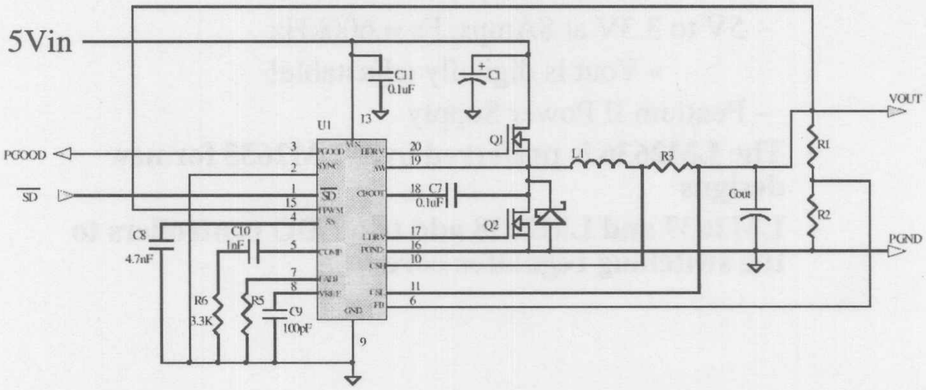
A non-synchronous conventional buck regulator can be built by ignoring the LSGATE signal.

The LM2637 and LM2638 use the same basic core switching regulator developed for the LM2636, but add two LDO controllers.

Lastly, these parts work great for powering Cyrix processors in desktop applications.

LM2631 Applications

- **5V to 3.3V at 3Amps, Fs = 500kHz**
- **5V to 2.5V at 6Amps, Fs = 300kHz**
- **5V to 3.3V at 8Amps, Fs = 300kHz**



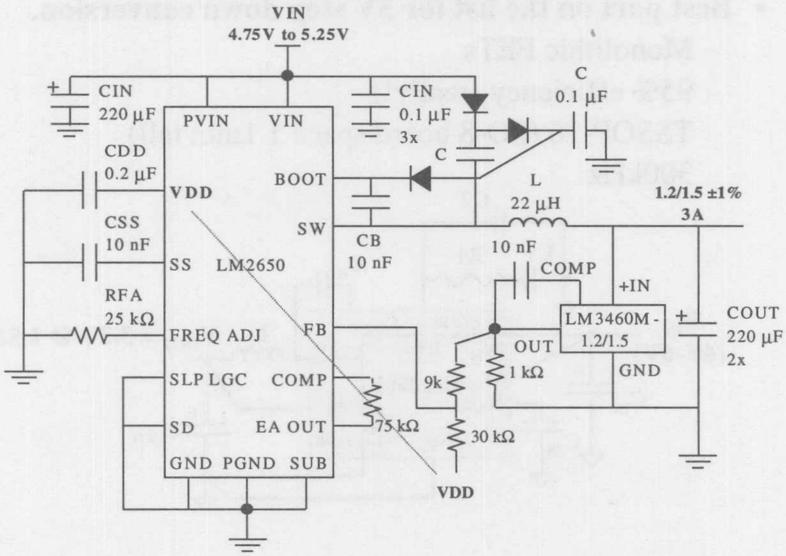
The LM2630 and LM2631 were designed as a notebook CPU core power supply controller. It is essentially a synchronous buck regulator with features making it suitable for battery powered applications. This means high efficiency over wide load ranges and uA shutdown currents. The LM2630 runs at 200kHz and the LM2631 runs at 300kHz.

The LM2630/1 has a input voltage range of 4.5 to 30V, so we can use it for 5V down conversion. In fact a number of customers have asked for these solutions, so this is our opportunity to share it with you.

These controllers are able to provide designs up to 8Amps. Above that current, the FETs gate capacitance gets so large that the controller simply can not effectively turn the FETs on and off.

The standard notebook CPU core voltage supply is also supplied in supplemental pages at the end of this section.

How Low Can You Go?
A Trick Demonstrated by the LM2650



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Analog Solutions 75

One of the most difficult types of low-voltage conversion is creating an output voltage of 1.2V or lower. This is lower than the 1.23-1.25Vinternal reference of the majority of ICs. The output voltage feedback is usually fed through an internal amplifier to take the difference of the feedback voltage and the reference. Since the amplifier is built to accept differences of 0V or greater, the minimum output voltage is normally equal to the internal reference voltage. So how can a 1.2V output be accommodated?

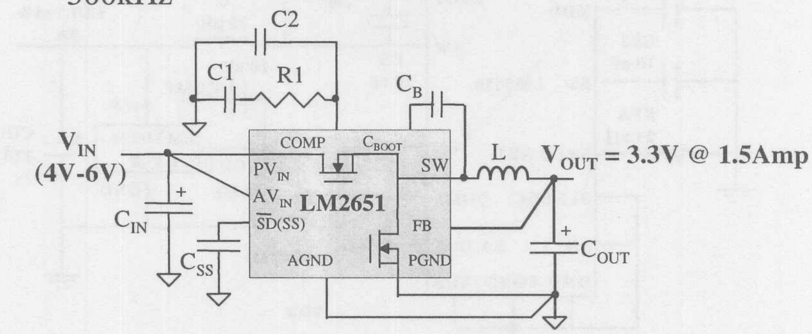
This trick is facilitated by having the VDD pin of the LM2650 available. VDD is a regulated internal 4V rail. If VDD was not available, we could generate it using a cheap reference.

Combining the power and efficiency of the LM2650 with the precision of the LM3460 voltage controller, we get a 1.2V or 1.5V output with low power loss. Because the LM2650 FB pin voltage needs to be at 1.25V, and the LM3460-1.2/1.5 output voltage range is 0 to 0.5V, the output voltage of the LM3460 must be level-shifted, using the 9k/30k network to the VDD pin of the LM2650.

Note the signal level diodes on the upper right of the schematic. If the input voltage is low (5V or less), the BOOT (bootstrap) function can't deliver enough gate voltage to fully drive the upper MOSFET on. This results in lower efficiency than is usually desired, as lower gate drive increases RDS(ON). By adding a switched-capacitor voltage doubler (via C1, C2, and three diodes), the voltage applied to the BOOT pin is double the input voltage; this improves the MOSFET gate drive, and the overall efficiency.

LM2651 - Monolithic Synchronous

- **Best part on the list for 5V step down conversion.**
  - Monolithic FETs
  - 95% efficiency (really!)
  - TSSOP-16 (SO-8 board space 1.1mm tall)
  - 300kHz



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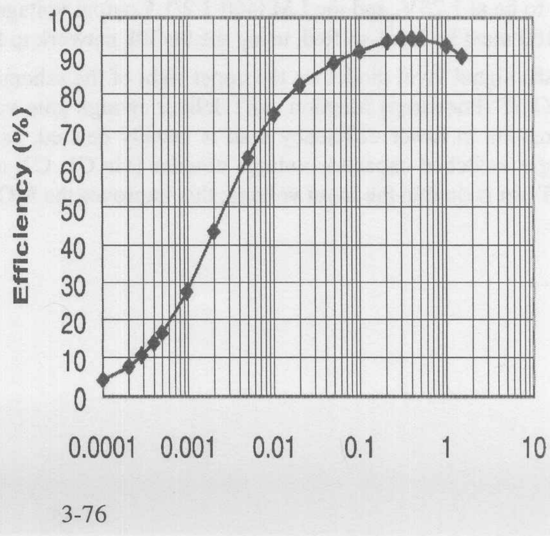
The LM2651 is the parent of the LM2653 you heard about earlier today. The LM2651 omits the power good flag and lock out features, but still retains the low power sleep and shutdown modes. It is available in the TSSOP-16 package. This is the first monolithic synchronous switching regulator in our 1.5micron Bipolar CMOS DMOS process.

This part does a fantastic job of converting 5V±20% down to 3.3V (minimum output is 1.5V). It does not require the voltage doubler like the LM2650 to get low on resistance of the upper FET. In fact, the LM2651 has 100mohm FETs which result in incredible efficiency. Just look at the graph below. This high efficiency also means very little generated heat. At 1.5Amps, only 0.55W is dissipated.

The operating frequency of 300kHz keeps components sizes small.

L1	10uF, Coilcraft DO3308P-103
C_{IN}	120uF, 6.3V, Sprague 594D
C_B	0.1uF ceramic capacitor
C_{SS}	4.7nF ceramic capacitor
C_{OUT}	150uF, 4V, Sprague 594D
C1	2.2nF ceramic capacitor
C2	100pF ceramic capacitor
R1	30kΩ, 5% resistor



Even More Solutions

- **30 years of power conversion**
  - LM100
- **Leaders in regulators and references.**
- **Call National for even more solutions to your power management and conversion needs.**

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The following 8 pages include even more solutions.

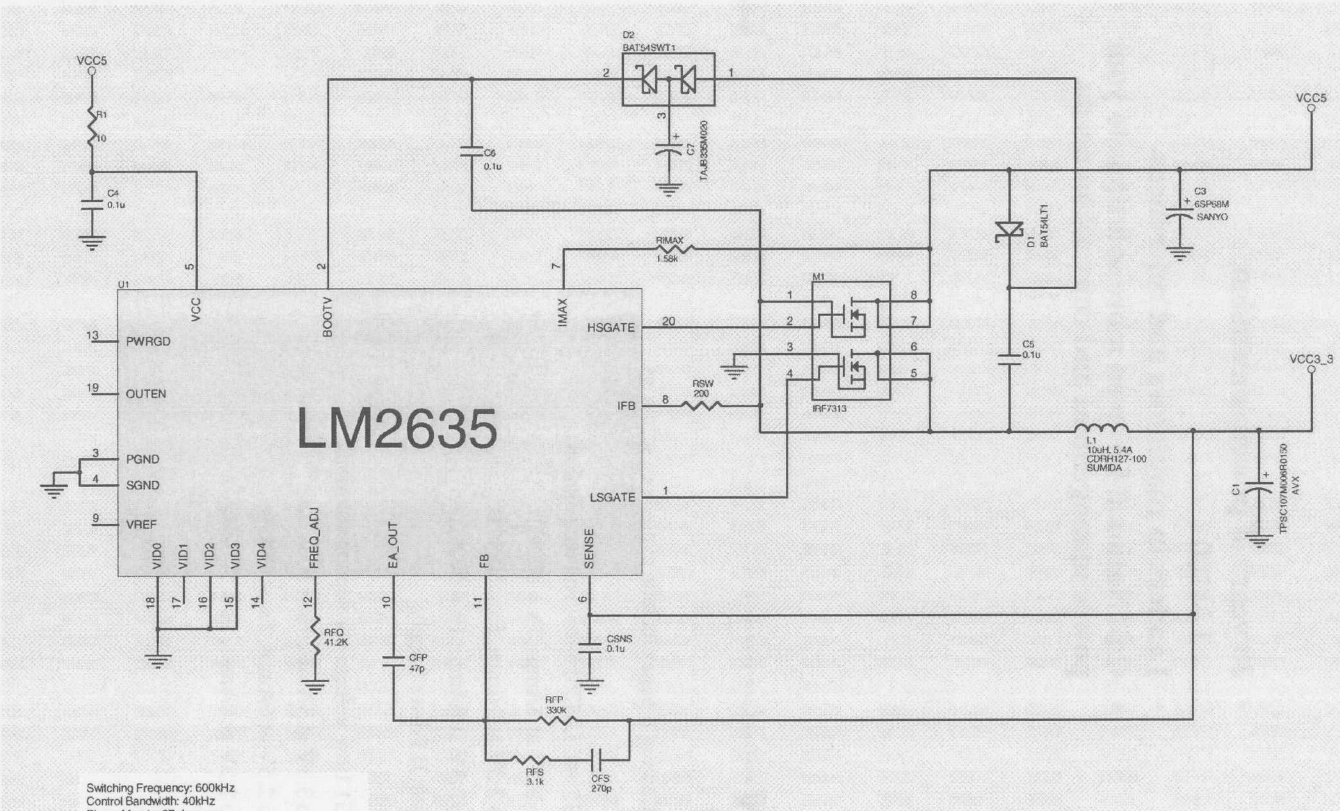
LM2635 and LM2636 low voltage solutions.

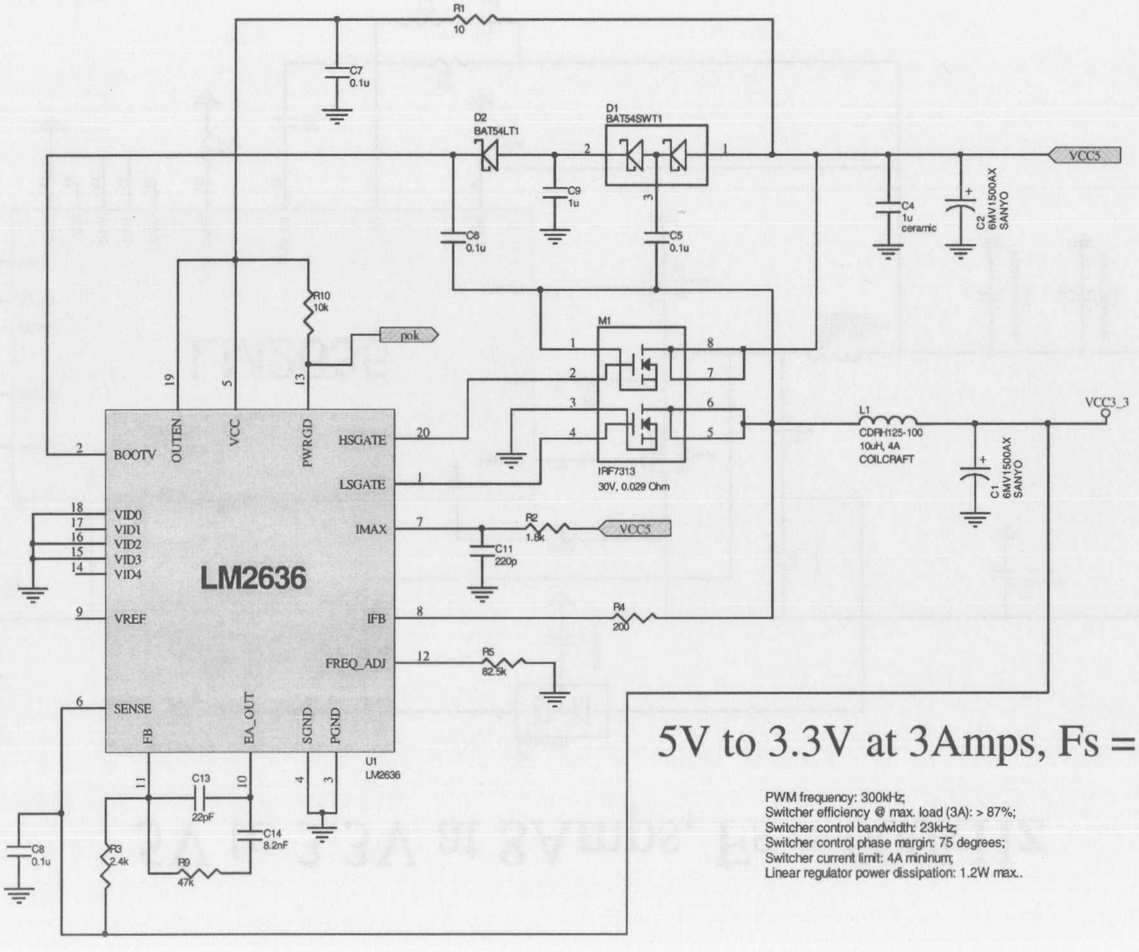
- 5V to 3.3V at 3Amps, Fs = 600kHz
- 5V to 3.3V at 3Amps, Fs = 300kHz
- 5V to 3.3V at 8Amps, Fs = 600kHz
- Pentium II Power Supply

LM2631 Low voltage conversion solutions

- 5V to 3.3V at 3Amps, Fs = 500kHz
- 5V to 2.5V at 6Amps, Fs = 300kHz
- 5V to 3.3V at 8Amps, Fs = 300kHz

5V to 3.3V at 3Amps, Fs = 600kHz

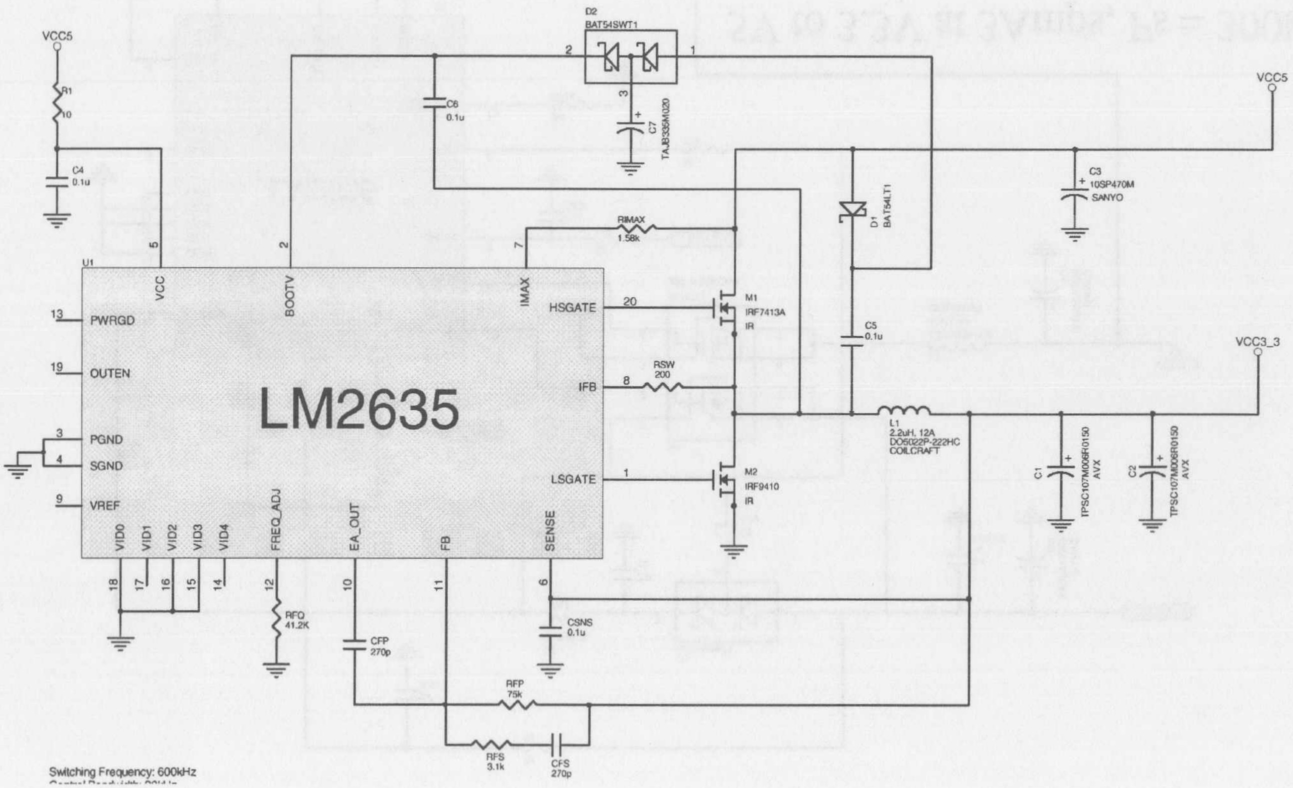




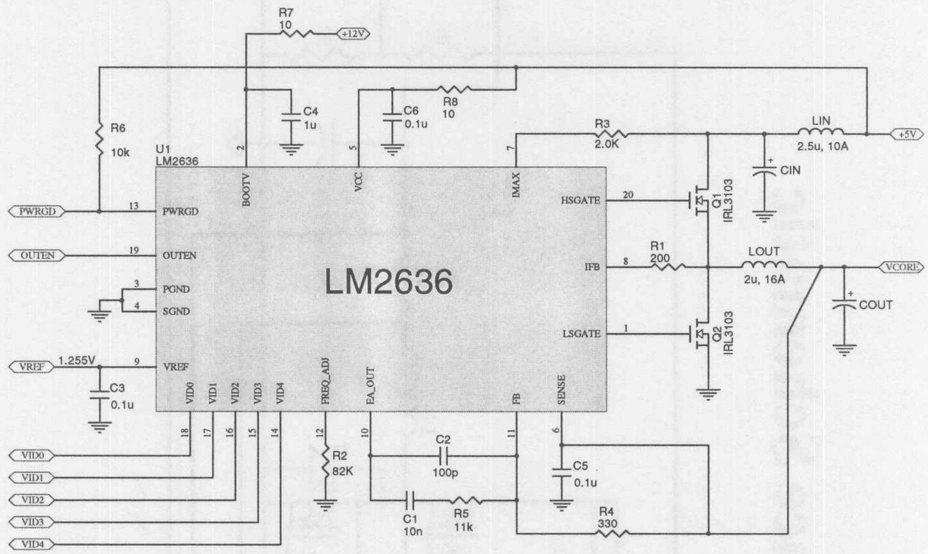
5V to 3.3V at 3Amps, Fs = 300kHz

PWM frequency: 300kHz;
Switcher efficiency @ max. load (3A): > 87%;
Switcher control bandwidth: 23kHz;
Switcher control phase margin: 75 degrees;
Switcher current limit: 4A mininum;
Linear regulator power dissipation: 1.2W max..

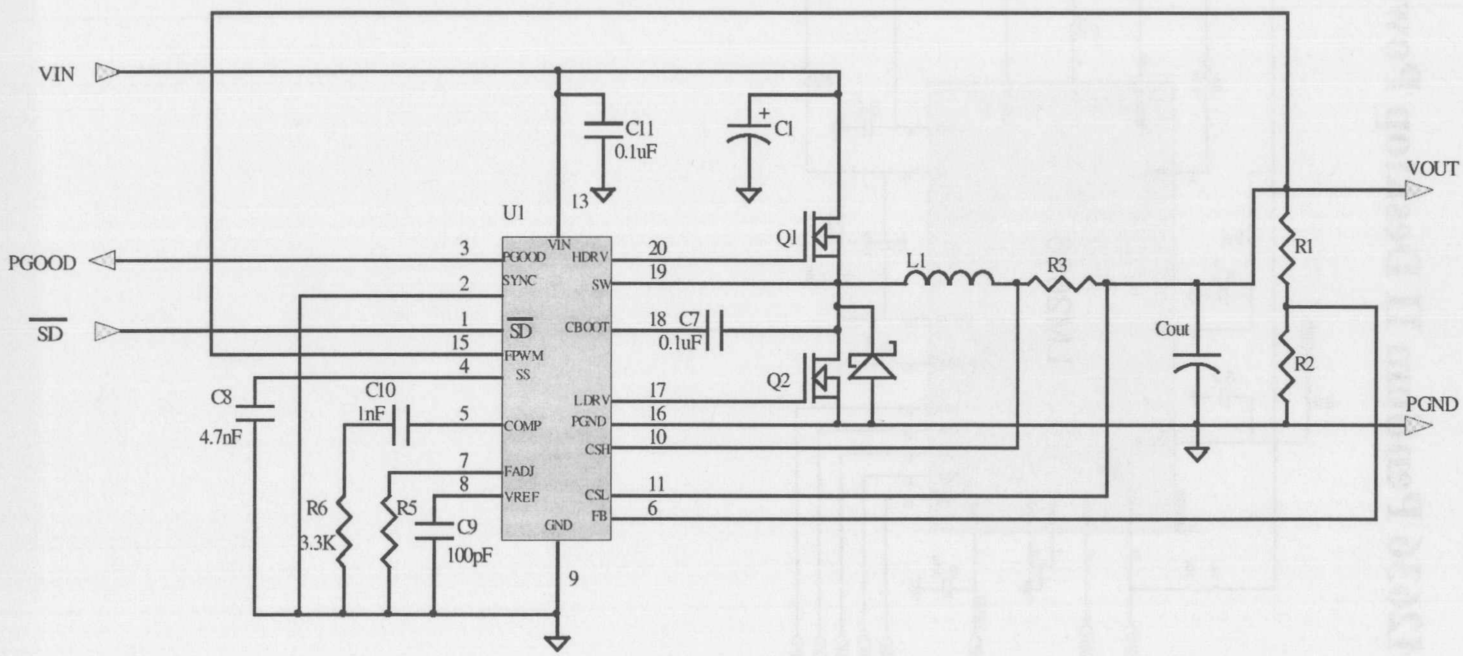
5V to 3.3V at 8Amps, Fs = 600kHz



LM2636 Pentium II Desktop Power Supply



LM2631 Reference Schematic



Bill of material (LM2631):
Iout(max)=6A, Vout =2.5V, Fs = 300kHz

Inductor ripple current: 1.2A peak to peak; Output voltage ripple: 40mV peak to peak.

Description	Part
Q1	IRF7807
Q2	IRF7807
Inductor L1	Sumida CDRH127-3R5, 3.5uH
Input Capacitors (Cin)	3 x 100uF, 10V AVX TPS or one Sanyo OS-CON 10SP470M
Output Capacitors(Cout)	3 x 220uF, 6.3V AVX TPS
Rectifier D1	Motorola MBRS140T3
Sensing Resistor R3	10mΩ IRC
Feedback Resistors R1 and R2	R1 = 10.2kΩ, 1%, R2 = 10kΩ, 1%
R5	348K
R6	3.3K
C7	0.1uF
C8	4.7nF
C9	100pF
C10	1nF
C11	0.1uF

Bill of material (LM2631):
Iout(max)= 3A, Vout =3.3V, Fs = 500kHz

Inductor ripple current: 0.22A peak to peak; Output voltage ripple: 22mV peak to peak.

Description	Part
Q1	NDS6680
Q2	NDS6680
Inductor L1	Sumida CDRH125-100, 10uH
Input Capacitors (Cin)	2 x 100uF, 10V AVX TPS or one Sanyo OS-CON 6SP68M
Output Capacitors(Cout)	220uF, 6.3V AVX TPS
Rectifier D1	Motorola MBRS140T3
Sensing Resistor R3	25mΩ IRC
Feedback Resistors R1 and R2	R1 = 16.9kΩ, 1%, R2 = 10kΩ, 1%
R5	275K
R6	3.3K
C7	0.1uF
C8	4.7nF
C9	100pF
C10	1nF
C11	0.1uF

Bill of material (LM2631): Iout(max)= 8A, Vout =3.3V, Fs = 300kHz

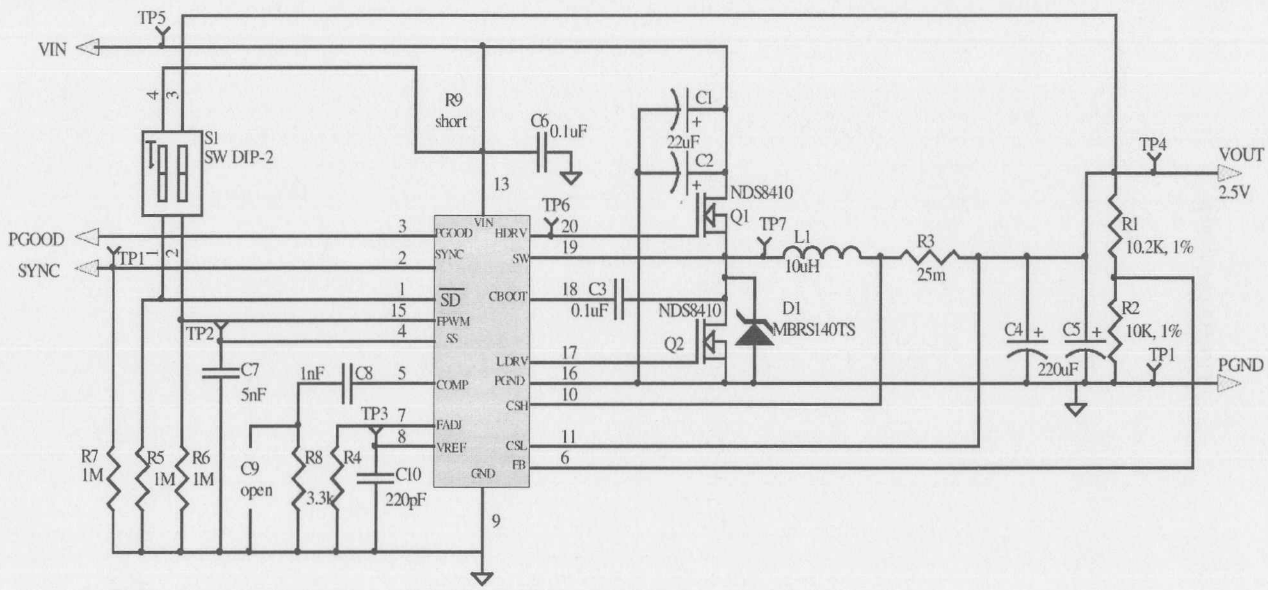
Inductor ripple current: 1.44A peak to peak; Output voltage ripple: 36mV peak to peak.

Description	Part
Q1	IRF7805
Q2	IRF7805
Inductor L1	Sumida EP169-2R6, 2.6uH
Input Capacitors (Cin)	3 x 100uF, 10V AVX TPS or one Sanyo OS-CON 10SP470M
Output Capacitors(Cout)	4 x 220uF, 6.3V AVX TPS
Rectifier D1	Motorola MBRD835L
Sensing Resistor R3	10mW IRC
Feedback Resistors R1 and R2	R1 = 16.9kW, 1%, R2 = 10kW, 1%
R5	348K
R6	3.3K
C7	0.1uF
C8	4.7nF
C9	100pF
C10	1nF
C11	0.1uF

Bill of material for LM2630/1 Notebook CPU Core Design:

Description	Part
Q1 and Q2	IRF7801
Inductor L1 Pulse	P0144, 9.4uH, 3.8A
Input Capacitors (C1, C2)	2 x 22uF, 35V AVX TPS
Output Capacitors(C4, C5)	2 x 220uF, 10V AVX TPS
Rectifier D1	Motorola MBRS140T3
Sensing Resistor R3	25mW IRC LR2010-01-R025
Feedback Resistors R1 and R2	R1 = 10.2kW, 1%, R2 = 10kW, 1% 1206 type
S1	DIP-2 switch: C&K BD02 (Digikey # CKN3001-ND) or Grayhill 78B02 (Newark #81F9139)
TP1-TP7 Terminals:	Cambion 160-1026-02-01 (can be found from Newark, Stock No. 40F6004)
R4	Open
R5, R6, R7	1M
R8	3.3K
R9	short
C3	0.1uF
C6	0.1uF
C7	4.7nF
C8	1nF
C9	Open
C10	220pF

LM2630/1 Notebook CPU Design



Note: Input capacitors (C_1 and C_2) and output capacitors (C_4 and C_5) are AVX, TPS capacitors.

Operation of the DIP-2 switch: when switch 1 is on, the device is in force PWM operation, when switch 1 is off, it is in hysteretic mode at light load; when switch 2 is on, the device is in normal operation mode, when switch 2 is off, it is in shutdown mode.

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ANALOG SOLUTIONS TRANSMISSION USING LVDS

WHAT IS LVDS?

L - Low

V - Voltage

D - Differential

S - Signaling

- **LVDS is a generic multi-purpose *Interface* standard for high speed / low power data transmission**
- **LVDS is standardized in the ANSI/TIA/EIA-644-1995 Standard**
- **National offers more than 60 LVDS products today, one for every application!**

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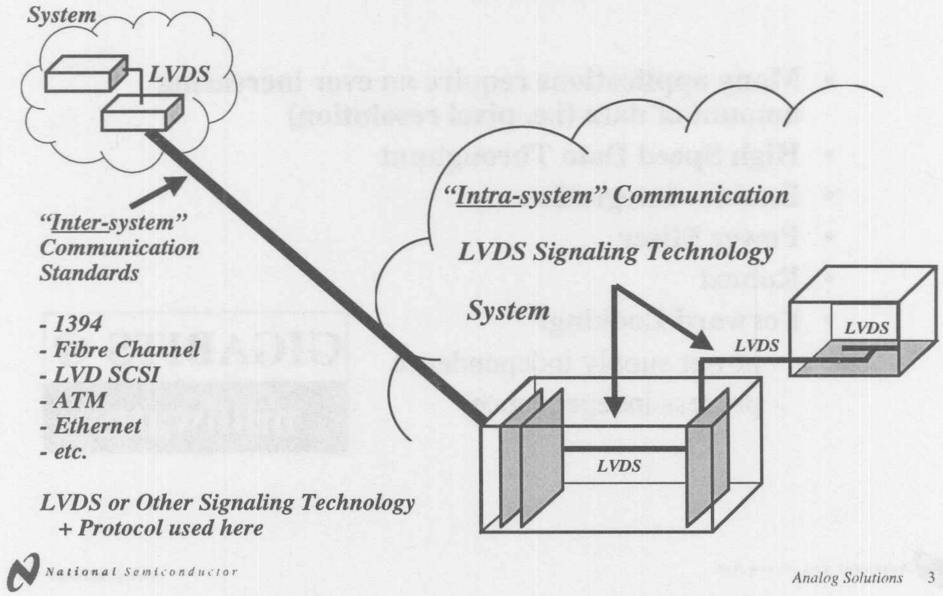
Analog Solutions 2

LVDS (Low Voltage Differential Signaling) is a generic multi-purpose interface standard for high-speed digital data transmission. It has been deployed in numerous applications spanning many market segments. These include:

Datacom:	Stackable Hubs
Telecom:	Wireless Base Stations, ATM Switches, ADD/DROP Muxs
Computing:	Flat Panel Displays, Servers
Peripherals:	Printers, Digital Copy Machines
Industrial:	High Resolution Displays
Automotive:	Flat Panel Displays

Where ever there is a need to transfer a vast amount of information, at high data rates (>100Mbps), LVDS offers a solution. The physical layer is standardized in the ANSI/TIA/EIA-644 specification. This standard defines driver and receiver electrical characteristics only. It does not define protocol, interconnect, or connector details. These are deemed application specific, and are to be referenced by the application requirements or referencing standard. This was done on purpose to ensure that LVDS becomes a generic multi-purpose interface standard.

WHERE IS LVDS USED?



LVDS is an electrical signaling technology used to convey 1's and 0's. Since high speed information needs to move into and throughout a system, there is a need to communicate this information to the outside world - intersystem - through an agreed upon protocol standard. This is what IEEE 1394, Fibre Channel, Gigabit Ethernet, etc. are used for today as well as others.

However, this information also needs to move THROUGH (i.e. within) a system and this is where National's LVDS solutions are mainly used today. Since the hardware and software overhead associated with the protocol solutions listed above are not always needed (and can be redundant and expensive) a simple, low cost LVDS link is used. Thus, National's LVDS solutions move information inter-system:

on a board,
board-to-board,
module-to-module,
shelf-to-shelf,
rack-to-rack,
or box-to-box across:

cables,
backplanes, or
PCB traces.

In the future, however, LVDS will be used with protocols for intersystem communication too.

WHY LVDS?

- **Many applications require an ever increasing amount of data (i.e. pixel resolution)**
- **High Speed Data Throughput**
- **Enables Integration**
- **Power Miser**
- **Robust**
- **Forward Looking:**
  - power supply independence
  - process independence

GIGABITS @
milliwatts

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Analog Solutions 4

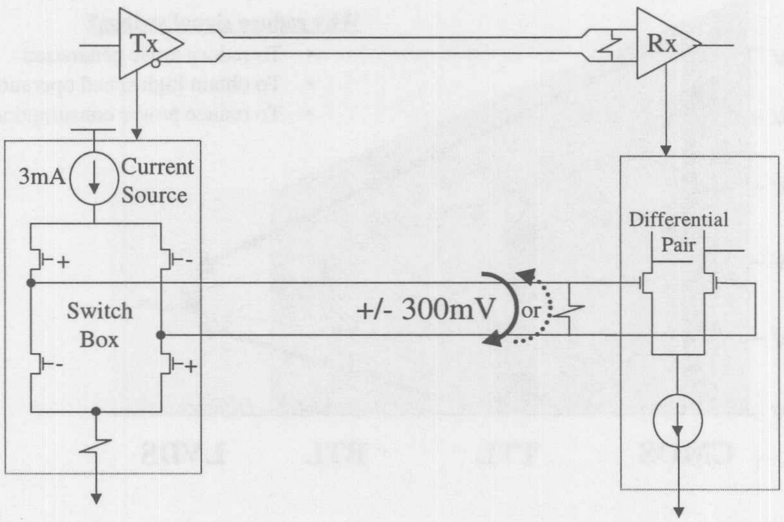
LVDS system benefits can be summed up in three words:

Gigabits at milliwatts!

LVDS provides an "easy to use" high speed interface for an ever increasing number of applications that require tremendous bandwidth. This technology is built from core CMOS and due to its' low power dissipation allows for deep (digital blocks) and wide (many channels) integration. Thus complete Interface Systems-on-a-chip are feasible today. Digital blocks that may be integrated include: DC Balance circuits, Clock Embedding, Clock Recovery, PLLs, Encoders, Decoders, Deskew, and many other digital functions.

Also, when the signaling levels were defined, the levels were chosen such that the drivers and receivers could be implemented in a wide range of technologies (Bipolar, BiCMOS, CMOS and even GaAs) and be powered from a wide range of power supplies (5V, 3.3V, 2.5V,…). This was done to ensure that LVDS will be the interface of choice for a number of generations to come.

HOW DOES LVDS WORK?



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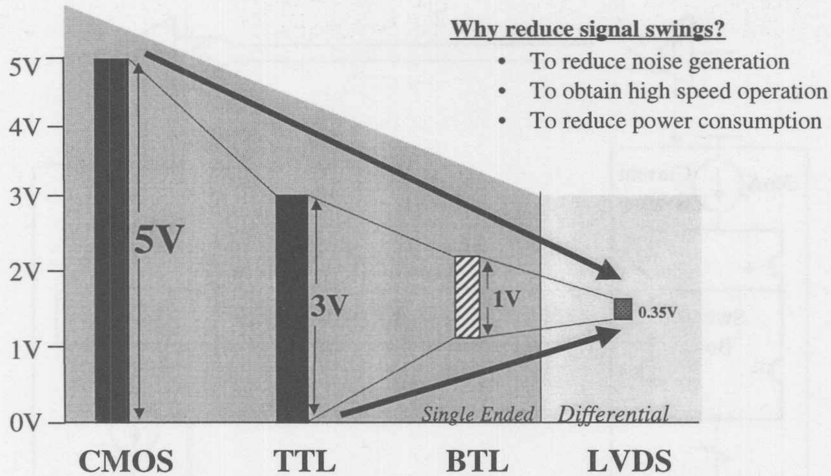
Analog Solutions 5

The LVDS driver equivalent output structure is shown above. Basically a current source limits output current to 3mA, and a switch box output steers the current to the load resistor that doubles as a termination resistor also. This differential driver uses odd-mode transmission with equal and opposite currents flowing in the line for the lowest amount of EMI generation. The current source also limits spike current that occurs during transitions, such that high data rates (100-1,000Mbps) can be supported without a substantial increase in power dissipation. The driver output is also very fault tolerant, and can tolerate shorts together or to ground without creating a thermal problem.

The receiver is a high impedance differential pair device, that detects very small (10mV) differential signals and converts them back into standard logic levels. The driven signal has a typical driver offset of +1.2V, and the receiver accepts a minimum input range of Ground to +2.4V. This allows for up to +/-1V of common mode rejection from noise picked up along the interconnect. Also with the input voltage range, hot plugging of LVDS receivers is possible. The receiver also has a failsafe feature to prevent output oscillations when the input pins are floating.

TECHNOLOGY TRENDS



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Analog Solutions 6

The use of TTL/CMOS Logic or reduced swing technology (BTL and GTL) for backplanes is today's common choice for design engineers, although they all lack the level of noise immunity that LVDS signaling offers, consume too much power, and suffer a lack of clear migration path.

To address higher speed applications signal swings have been reduced. However noise margins are reduced as well. To solve this problem LVDS and BLVDS uses differential data transmission to double the noise margin while reducing the swing even more.

HOW DOES LVDS COMPARE?

Parameter	*LVDS*	*TTL/CMOS*	*GTL/BTL*	*PECL*
Signaling	Differential	Single Ended	Single Ended	Diff / SE
Output Voltage Swing	± 300mV	2.4-5.5V	1V	± 800mV
Receiver Threshold	±100mV	1.2/1.5V	±200mV	± 200mV
Maximum Speed [1]	>400Mbps	<100Mbps	<100Mbps	>400Mbps
Drive Current mA [2]	3mA or 10mA[3]	75mA	40-80mA	40-60mA
Noise Generation	Low	High	Medium	Medium
Power Dissipation	Ultra Low	High	Med. - High	Medium

[1] Configuration, device and application dependant - general estimate given for NON - MUXed devices (simple level translator - i.e. DS90LV047A)

[2] Drive to switch bus. GTL depends on "vendor flavor"

[3] Bus LVDS output drive current is 8-10mA

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Analog Solutions 7

LVDS is commonly compared to other technologies. The above chart highlights basic electrical comparisons and also some generic system parameters.

KEY SPECIFICATIONS OF LVDS
ANSI/TIA/EIA-644-1995 Standard

Driver Differential Output Voltage	**Vod**	**250-450 |mV|**
Driver Offset Voltage	**Vos**	**+1.25 V**
Receiver Thresholds	**Vth**	**± 100 mV**
Receiver Input Voltage Range	**Vin**	**GND to + 2.4 V**
Common Mode Range	**Vcm**	**± 1V around 1.25 V**
Differential Noise Margin	**DNM**	**150 mV**
Data Rate Range	**f**	**DC to ≥655 Mbps**
Cable Length Range	**l**	**0 to ~15 meters**

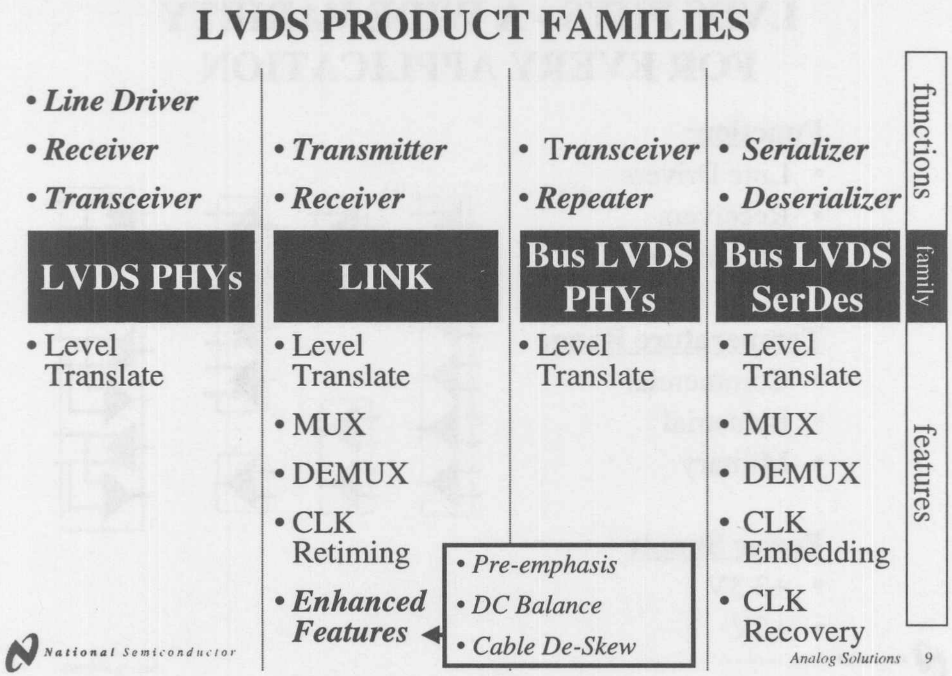
National Semiconductor *Analog Solutions* 8

As mentioned earlier, the ANSI/TIA/EIA/644 standard defines the electrical parameters of the interface only. The table above highlights the major parameters for standard LVDS devices.

The driver features a small differential swing of typically +/-300mV, offset from ground by +1.25V. The receiver detects an input of +/-100mV over the common mode range of Ground to +2.4V. This supports a +/-1V of common mode rejection for noise tolerance. A small differential noise margin is also provided: 150mV (VODmin - VTH => 250 - 100 = 150mV). This is small but adequate. Traces connecting the drivers and receivers should be closely-coupled, and twisted pair cables should be employed. This helps to ensure that all noise picked up along the cable is coupled equally to both lines of the pair and rejected by the receiver(s) as common mode.

LVDS parts are capable of very high data rates. The signaling rate can easily exceed 655 Mbps, and into the Gigabit range. Maximum switching rate is device, and interconnect dependent.

Since LVDS provides a +/-1V common mode range, interconnect media should be short hauls in the "few meters" to "10s of meters" in length.



National offers a wide range of LVDS products for many different application needs. These are currently classified into four different families.

LVDS PHYs provide simple level translation from LVTTL/CMOS to LVDS and back. Line Driver, Receiver, and Transceiver functions are currently offered. These devices tend to operate in the 100 to 400 Mbps range, mostly depending upon how fast data can be delivered to them by the logic device before the LVDS line driver.

The LINK family increases line speed and throughput with the integration of MUX and DEMUX circuits to collect seven slow speed parallel TTL lines and serialize (deserialize) them into high speed LVDS channels. Also integrated into these chips are PLL circuits that control the interface timing and data recovery. Two sub families are offered today:

FPD-Link for LCD Display applications, and

Channel Link for generic bus applications.

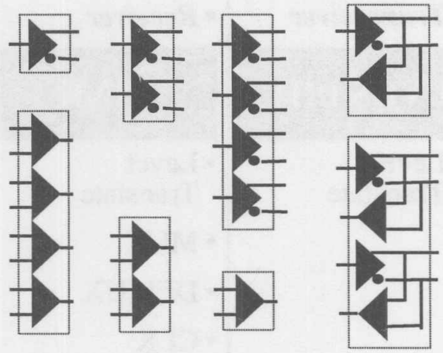
The Bus LVDS family was introduced in the Summer of 1998, and provides an enhanced output to enable multi-point applications which require two terminations (one at each end of the bus).

The Bus LVDS PHYs are similar to the LVDS PHYs, and translate between standard logic levels and BLVDS levels.

The Bus LVDS SER/DES family are complex Communication Systems-on-a-chip devices. They serialize / deserialize a 10 bit word and embed the clock at data rates up to 400Mbps. These can be used in point-to-point, multi-drop, and multi-point applications.

LVDS PHYS - A WIDE VARIETY FOR EVERY APPLICATION

Function:
- Line Drivers
- Receivers
- Transceivers



Temperature Range
- Commercial
- Industrial
- Military

Power Supply
- +3.3V
- +5V

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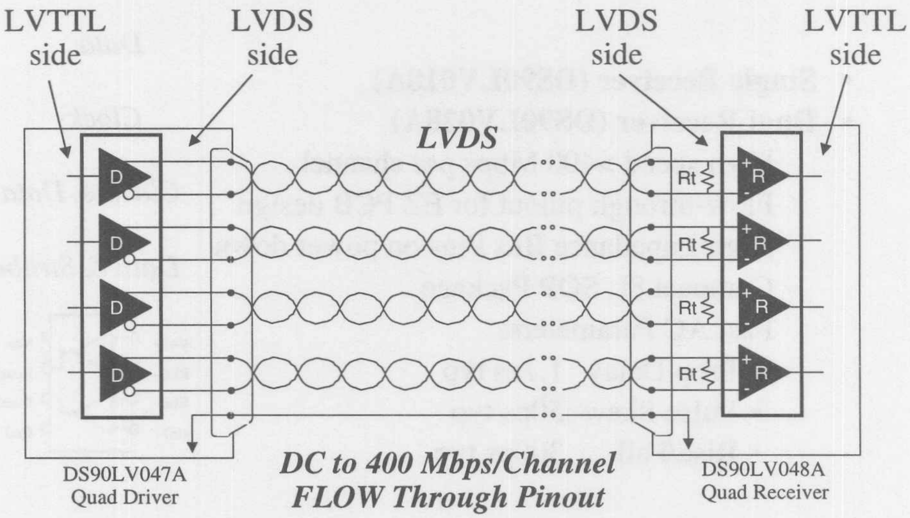
Analog Solutions 10

Sixteen different simple LVDS PHYs are currently offered. These are available in single, dual, or quad pinouts and support both Line Driving, and Receiving functions. Transceiver functions are also available. Commercial, Industrial, and even Military temperature ranges and 3.3V or 5V parts are available. For specific configurations, please refer to the National LVDS Feature page at:

www.national.com/appinfo/lvds/

or see our selection guide on LVDS INTERFACE (LIT# 550064-002).

NEW QUAD PIN OUT EASES PCB DESIGN



DC to 400 Mbps/Channel
FLOW Through Pinout

National Semiconductor *Analog Solutions* 11

The brand new DS90LV047A QUAD LVDS LINE DRIVER and companion DS90LV048A QUAD LVDS RECEIVER provide an enhanced pinout to simplify PCB layout. In high speed busses, it is important to minimize length differences between channels, and also the electrical length of the lines within a pair should be matched to minimize EMI generation. The 047 & 048 provide the LVDS Bus Pins on one side of the package, and the LVTTL pins on the other. This greatly eases PCB trace layout, and helps to isolate noisy single-ended signals for the high speed small swing LVDS I/O lines. These products are rated at 400Mbps, and offer faster AC parameters and very low skew.

VERSATILE SINGLE & DUAL RECEIVERS

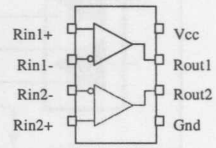
- **Single Receiver (DS90LV018A)**
- **Dual Receiver (DS90LV028A)**
  - High speed >400 Mbps per channel
  - Flow-through pinout for EZ PCB design
  - High Impedance Bus Pins on power down
  - Compact 8L SOP Package
  - Fast AC Parameters:
    - Prop Delay 1.7ns typ
    - Pulse Skew 50ps typ
    - Rise/Fall 300ps typ

Data

Clock

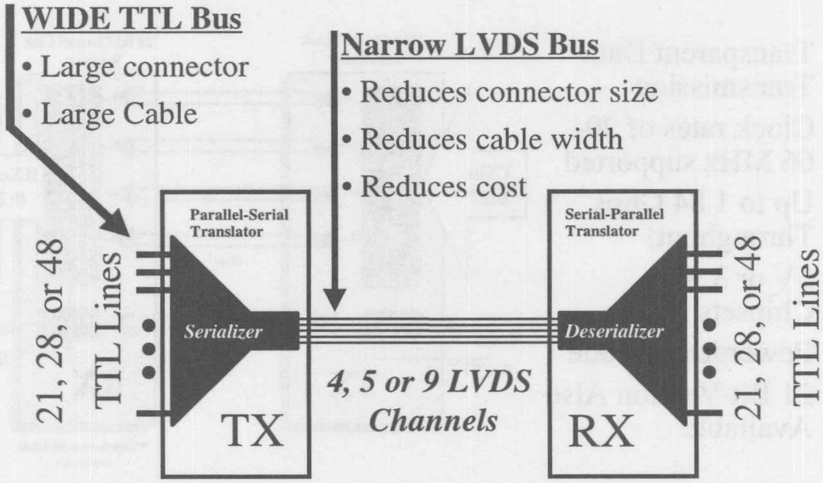
Clock & Data

Data & Strobe



Two other new members of the LVDS PHY family are the single and dual receivers. These also offer a flow through pinout to ease PCB design, and screaming AC performance for 400Mbps service. The parts are very versatile, and can be used for a single data channel, Clock driving, and the dual receiver can be used for a Clock / Data or Data / Strobe application.

REDUCE INTERCONNECT WITH LVDS CHANNEL LINK



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The LINK Family unleashes the throughput potential of LVDS while offering a GREAT system savings! MUX/DEMUX and retiming functions have been added to the chipset in addition to the level translation function. This breaks the TTL bottleneck on speed and each LVDS data channel serializes 7 slow TTL lines into a single high speed LVDS line with operation up to 700Mbps (device specific).

Besides the throughput, the reduction in interconnect provides multiple benefits to the system, including:

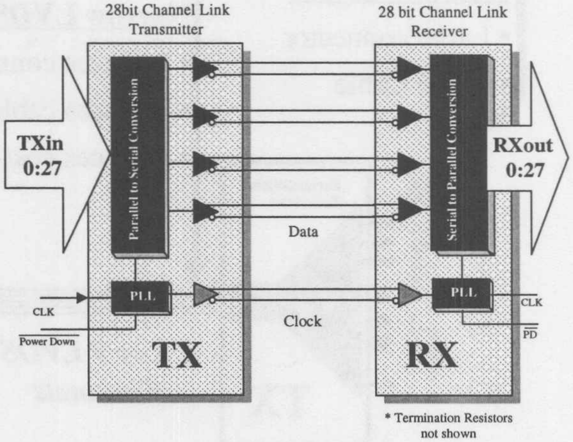
The required cable is smaller, more flexible, and lower cost!

The required connector has less pins, is smaller, and again lower cost!

Depending upon the system and application, a reduction of up to 80% of the interconnect size is possible, yielding great cost savings.

28 BIT BUS SQUEEZE REDUCES INTERCONNECT COST

- Transparent Data Transmission
- Clock rates of 20-66 MHz supported
- Up to 1.84 Gbps Throughput!
- 5V or 3.3V Chipsets
- Powerdown Mode
- 21 Bit Version Also Available



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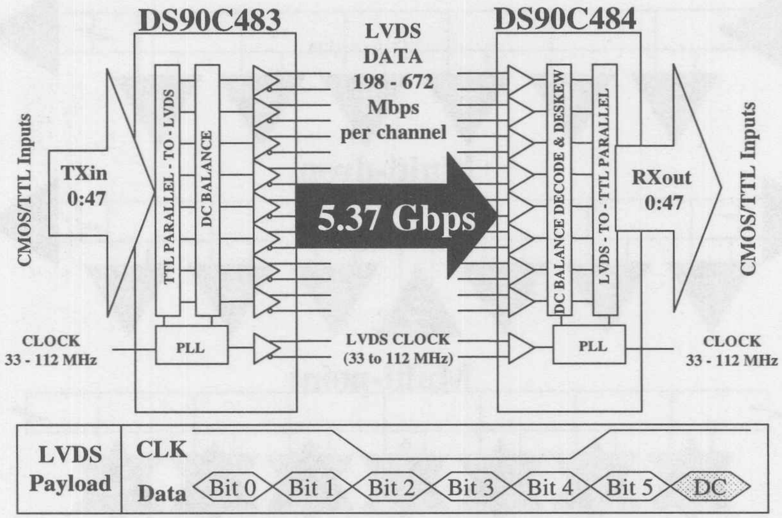
Analog Solutions 14

The Channel Link chipset is offered as a 21 bit part that serializes to 3 data pairs plus clock, or as a 28 bit chipset that serializes to 4 data pairs plus clock (shown above). Both 5V and 3.3V parts are offered, and clock speeds up to 66MHz are currently supported. Higher speed parts will be offered shortly, so for the latest product information, check our web site at:

www.national.com/appinfo/lvds/

48 BIT BUS SQUEEZE PROVIDES 48:9 COMPRESSION



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Analog Solutions 15

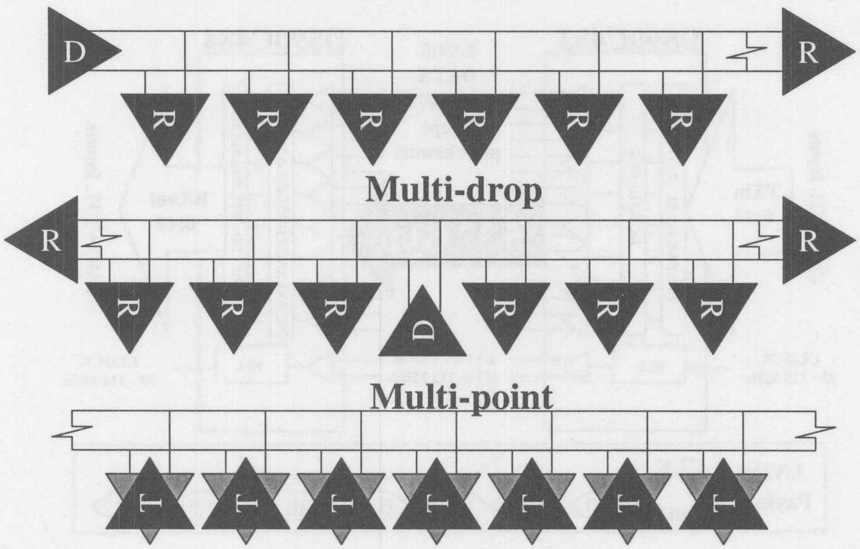
The newest Channel Link chipset supports a TTL data bus up to 48 bits wide and clock rates up to 112MHz. With 48 inputs and a 112MHz clock, **an impressive 5.37Gbps throughput is obtained!** This chipset is also enhanced with extra features to extend the cable length of the interconnect. The Transmitter has two new features:

Pre-emphasis is user selectable, and provides additional dynamic current during transitions to open up the signal eye, and eliminate cable distortion effects to the signal.

DC Balance is also provided on a frame by frame basis. The 7th LVDS data bit indicates whether the data in the payload is "true" or has been "inverted" to maintain equal charge on the cable. This also helps to keep the signal eye wide and open at the receiver end.

The receiver has a new **Deskew** feature built in. This feature deskews the pair-to-pair skew caused by long cable interconnects up to +/- 1 bit time to ensure correct data recovery.

BUS LVDS SUPPORTS MULTI-DROP AND MULTI-POINT APPLICATIONS!



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Analog Solutions 16

Bus LVDS was developed to service double termination applications. It is an extension of LVDS which is primarily intended for simple point-to-point applications or multi-drop applications. Both of which employ a single termination at the far end of the cable, and a single driver at the near end. This is shown above in the top diagram where a single driver is connected to one or more receiver loads, and a single termination resistor is used at the far end of the cable.

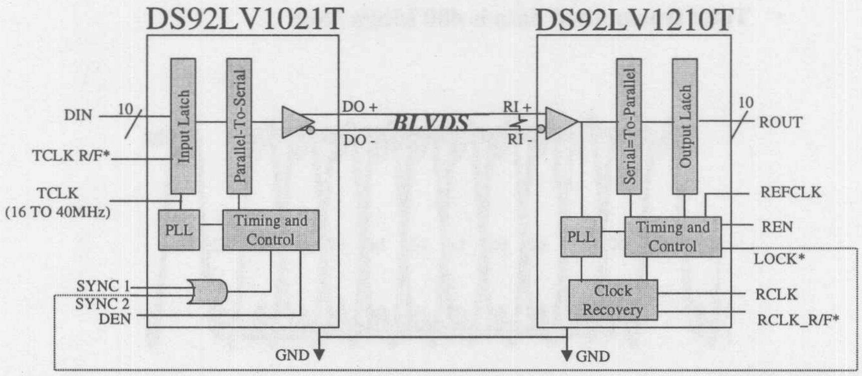
An alternate application is shown in the middle, with the driver located in the center of the bus. Receiver loads are located on both sides, and termination is required at both ends to prevent reflections. Standard LVDS drivers do not support this configuration, as the double load would be seen in parallel to the driver, and the differential output voltage would be cut in half (150mV which is deemed too low). Bus LVDS drivers provide 8-10mA of output current, so that they can provide "LVDS" type signaling even with low impedance loads. The middle application is also of use when the flight time from source to destination needs to be minimized, as it is 1/2 that of the top configuration.

The lower configuration is the wild card multi-point bus, that is typical of a shared backplane bus. (Note: T = Transceiver) All nodes are capable of either driving or receiving data, but only one driver may be active at any given time. This application also requires termination at both ends, since the source location is not known.

The Bus LVDS family supports all three configurations! For simple PHY functions, a single transceiver, a Nine Channel Transceiver and a repeater device are currently offered. Details on these devices can be found on the LVDS web page.

10 BIT SERIALIZER / DESERIALIZER CHIPSET EMBEDS CLOCK

- **Bus-able driver outputs for dual termination loads**
- **Reduces interconnect size and cost**
- **Provides clock embedding and recovery functions**

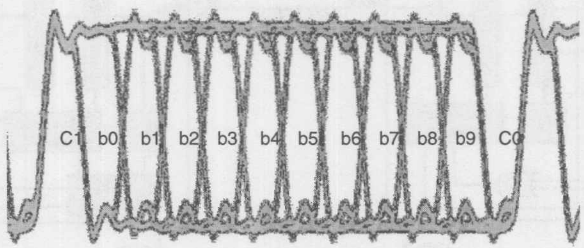


The newest members of the Bus LVDS family are the Serializer and Deserializers. The block diagram is shown above for the DS92LV1021 and standard receiver DS92LV1210. These parts support clock rates from 16 to 40MHz and serialize a 10 bit (8 data, 1 parity, 1 frame) into a single BLVDS data channel. The clock is also embedded and recovered by the chipset. This is a versatile chipset, and configuration pins to select data strobe edge are also provided along with a power down function.

This chipset may be used in point-to-point applications, or multi-drop distribution systems as shown on the prior slide. Multi-point is also possible with certain considerations of loading, spacing, and turn around (PLL Lock) time.

400 MBIT/S PAYLOAD

- **10 bits are sent every TCLK cycle**
  - 10 * 40 MHz = 400 Mbits / Sec
- **2 clock bits added for deserializer clock recovery**
  - 2 * 40 MHz = 80 Mbits / Sec
- **Total transmitted data is 480 Mbits / Sec**



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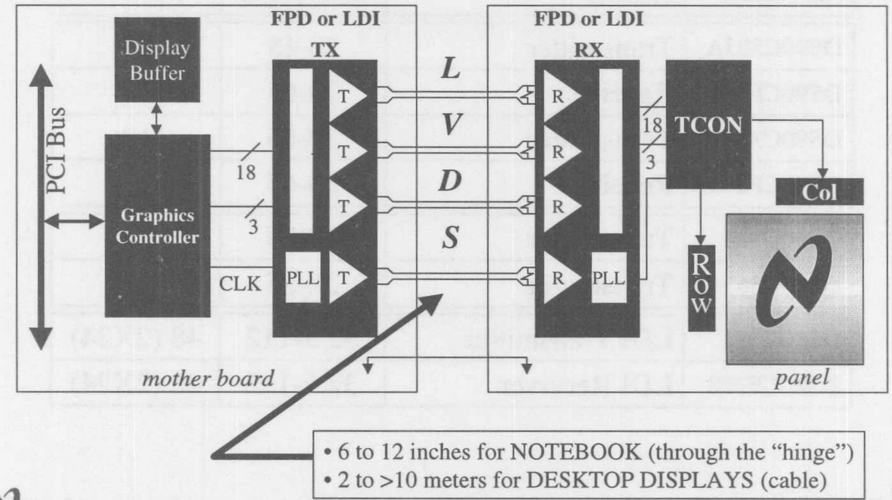
Analog Solutions 18

This slide illustrates the chipset's payload with the 10 bits of information and two embedded clock bits.

Actual transfer rate with a 40MHz clock is 480 Mbps, and the throughput (information rate) is 400Mbps. The embedded clock edge is used by the receiver to lock to the inbound serial stream and for data alignment purposes. This chipset can be run across short cable hops or across backplanes. It provides similar system benefits as with the LINK family in reducing interconnect size and cost.

ENABLE HIGH RESOLUTION FLAT PANELS WITH FPD-LINK & LDI



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Analog Solutions 19

FPD-Link (Flat Panel Display Link) is primarily targeted at LCD applications for Notebook and Sub-Notebook applications. It takes the wide RGB (Red/Green/Blue) bus of 18 or 24 bits along with three control lines (VSYNC, HSYNC, and Data Enable) and MUXes them down to only 4 or 5 pairs. This small interconnect is then passed through the hinge from the motherboard to the panel, and then DEMUXed. Typical interconnects are twisted pair wires or flex circuit interconnects, and range from a few inches to about 16 inches in length.

LVDS interfaces are required on XGA resolution panels and above (they are also used on many SVGA Panels as well) due to the bandwidth requirements.

The newest LVDS Panel Chipset is called LDI (LVDS Display Interface) and is for desktop monitor applications. This chipset supports 24 bit color and provides over **5Gbps** throughput across 8 data pairs and cable lengths up to 10 meters. The LDI Chipset also supports the use of Pre-emphasis, DC Balance, and Cable Deskew to extend the reach of FPD-Link to monitor applications with long cable interconnects.

FPD-Link & LDI CHIPSETS

Part Number	Function	Clock (MHz)	RGB Bits
DS90C383A	Transmitter	20-65	24
DS90CF384A	Receiver	20-65	24
DS90C363A	Transmitter	20-65	18
DS90CF364A	Receiver	20-65	18
DS90C385	Transmitter	20-85	24
DS90C365	Transmitter	20-85	18
DS90C387	LDI Transmitter	32.5-112	48 (2X24)
DS90CF388	LDI Receiver	32.5-112	48 (2X24)

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Analog Solutions 20

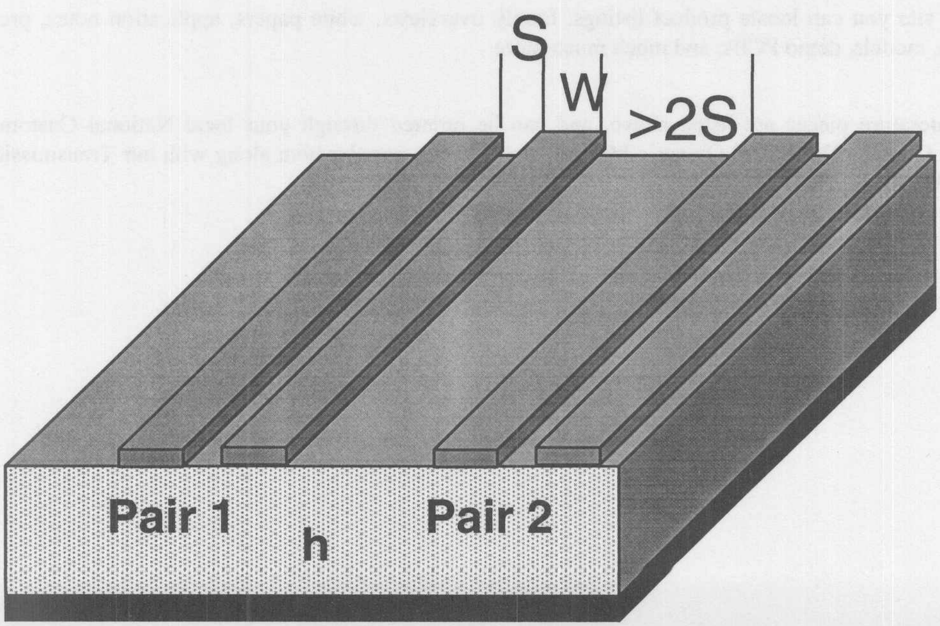
This slide shows a partial listing of the FPD-Link and LDI chipsets. It lists the latest generation 3.3V devices. The 65MHz parts support SVGA and XGA applications. The 85MHz parts support reduced blanking SXGA, XGA and SVGA applications. The LDI chipset supports SVGA to QXGA high resolution applications!

DESIGN TIPS FOR LVDS

- Hand route or review auto-route differential pairs carefully
- Locate I/O devices as close to connector as possible
- Calculate and optimize differential traces (not 2X 50 Ohm)
- Place adjacent differential pairs at least 2S away
- Place TTL signals at least 3S away or isolate on a different layer
- Match electrical length of differential lines
- Avoid crossing slots in ground planes
- Avoid 90 degree bends (use two 45s)
- Minimize the number of via on a line (layer transitions)
- Preserve balance (equally load both lines)
- Match connector impedance on in-line connectors to interconnect
- Terminate with 2% surface mount resistors
- Use 4 or more layer PCBs
- Use good bypassing on the PCB (Bulk and High Frequency)

SEE AN-905, AN-1085 and AN-1108 for more details!

The above slide provides the generic recommendations for high speed LVDS PCB design. Please see also National application notes: AN-905, AN-1085, and AN-1108 for much more detailed recommendations. In the above bullet list, the term "S" refers to the distance between the lines that make up the differential pair. This is further illustrated in the graphic below that would not fit on the slide:



DESIGN TOOLS

- LVDS WWW Feature Site:
  http://www.national.com/appinfo/lvds/
- LVDS Owner's Manual *LIT# 550062-001 (Spring 1997)*
- **High Speed Interface Selection Guide (LVDS/BLVDS/SDI)** *LIT#550064-002*
- *RAPIDESIGNERS for Transmission Line Calculations*
  (see web site at http://www.national.com/appinfo/lvds/*)*
- LVDS Application Notes
  (see web site at http://www.national.com/appinfo/lvds/*)*
- *NEW* 1999 Interface Databook *LIT# 400058*

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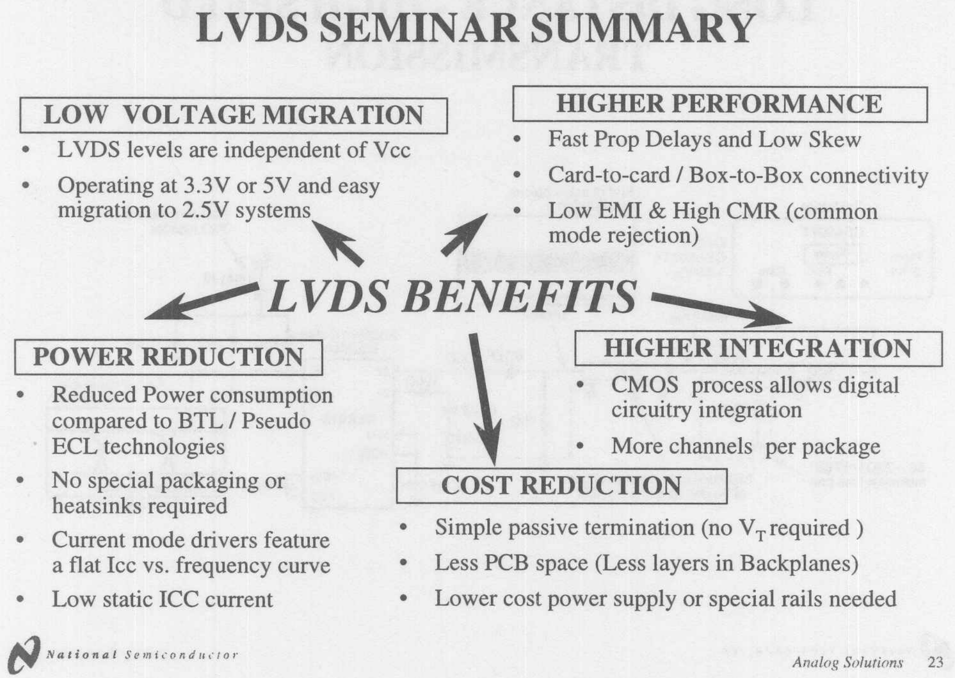
A wide range of tools and applications material is available from National on LVDS. The most current one-click location is our feature site on LVDS at:

www.national.com/appinfo/lvds/

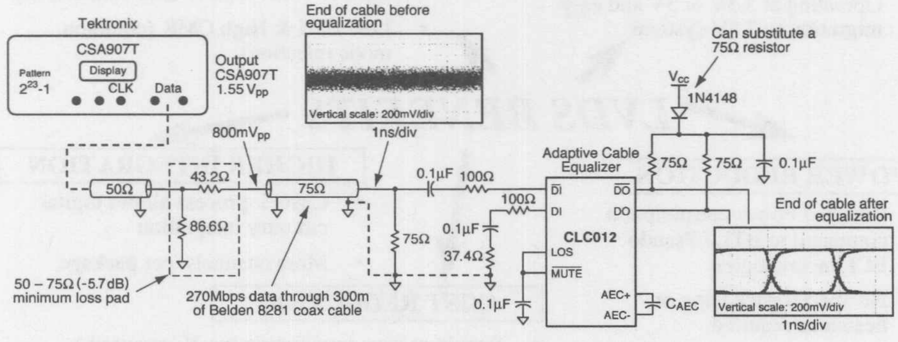
On this site you can locate product listings, family overviews, white papers, application notes, press releases, models, demo PCBs, and much much more.

Other literature pieces are listed above, and can be ordered through your local National Customer Support Center. The LVDS Owner's Manual is also a very popular item along with our Transmission Line RAPIDESIGNERs.



This slide provides an overview of the many benefits that LVDS and Bus LVDS provide to your applications.

LONG DISTANCE - HIGH SPEED TRANSMISSION



If you need high speed transmission **AND** long distance too, then we also have a solution for you!

The slide shows a typical measurement system for evaluating the CLC012 Cable Equalizer. Data can be recovered after 300 meters of coax cable through the use of the new CLC012 Equalizer.

The above slide illustrates a typical test set up. The output of the CSA907 PRBS is adjusted to provide 800mVpp at the transmit end of the cable. The minimum-loss pad equalizes the impedance level from the 50Ω output of the PRBS to the 75Ω input at the CLC012. There is a signal attenuation of 5.7dB in the MLP.

The scope shows the attenuated signal before and after 300m of cable.

The CLC012 Adaptive Equalizer provides the necessary amplitude equalization to boost the signal to an ECL output level. In an actual application, the CLC005 driver should be used in place of the test generator (CSA907).

This chipset operates from 50Mbps to 622 Mbps over great distances.

SERIAL DIGITAL INTERFACE PRODUCTS

Part Number	Function	Data Rate Mbps	Typ Jitter - ps
CLC005A	Single Cable Driver	Up to 622	25
CLC006A	Single Cable Driver	Up to 400	25
CLC007A	Cable Driver w/Dual Outputs	Up to 400	25
CLC0011B	SDV Decoder	Up to 360	50
CLC012A	Cable Equalizer	50 to 622	150
CLC014A	Cable Equalizer	50 to 650	180
CLC016A	Retimer	40 to 400	130
CLC018A	8X8 Crosspoint	Up to 1,400	50

HIGH Speed - Long Distance (100-300+ meters) - LOW Skew

National Semiconductor *Analog Solutions* 25

This slide lists the other members of the Serial Digital Interface (SDI) product family offered by National.

It is commonly used in SDV (Serial Digital Video) applications conforming to SMPTE standards.

It is also commonly used in telecom applications at 155 or 622Mbps over coax or twisted pair (CAT 5) cables.

This chipset may also be employed where ever there exists a need to transmit data over great distances. For more information on this family of High Speed Interface parts, please visit our other interface web site at:

www.national.com/appinfo/interface/

COMMUNICATE WITH RS-232 SERIAL PORTS

- **Drivers**
  - DS1488, Quad Line Driver
  - DS14C88, Quad CMOS Line Dr.
  - DS75150, Dual Line Driver
- **Receivers**
  - DS1489/A, Quad Line Receiver
  - DS14C89A, Quad Line Receiver
  - DS75154, Quad Line Receiver
  - DS9627, Dual Line Receiver
- **Drivers/Receivers (3x5)**
  - DS14185, 3 Drs. X 5 Rcrs.
  - DS14C335, 3 Drs. X 5 Rcrs. Shutdown, Single Supply Vcc=3.3V
  - DS14C535, 3 Drs. X 5 Rcrs. Shutdown, Single Supply Vcc=5V

Drivers/Receivers (5x3)

DS14196, 5 Drs. X 3 Rcrs.
DSV14196, 5 Drs. X 3 Rcrs. Low Voltage Vcc = 3.3V (NEW)

Drivers/Receivers (2x2)

DS14C232, 2 Drs. X 2 Rcrs. Single Supply Vcc = 5V

Drivers/Receivers (4x4)

DS14C238, 4 Drs. X 4 Rcrs. Single Supply Vcc = 5V

Drivers/Receivers (4x5)

DS14C241, 4 Drs. X 5 Rcrs. Shutdown, Single Supply Vcc=5V

National Semiconductor *Analog Solutions* 26

Recommended Standard (RS) interface products are also available from National. The slide above list the currently available RS-232 devices by configuration. The newest device is the DSV14196 which provides 5 drivers and 3 receivers with a 3.3V logic side interface.

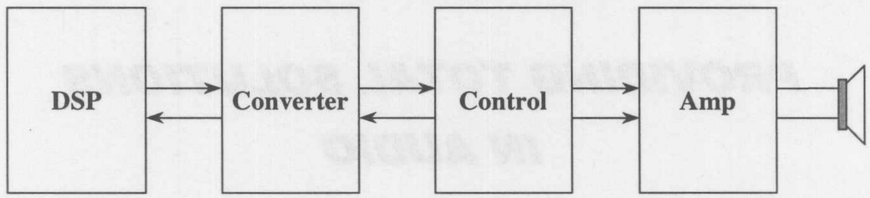
RS-422, RS-423, and RS-485 devices are also offered. Selection Guides and applications information can be located at:

www.national.com/appinfo/interface/

National *Semiconductor*

PROVIDING TOTAL SOLUTIONS IN AUDIO

The Audio Chain
Progress in providing the "total" solution



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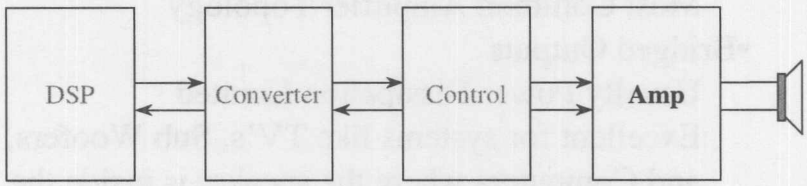
Analog Solutions 2

National has been involved in supplying monolithic Audio solutions for over twenty five years. The applications included such things as diverse as Pachinko machines, toys, Automotive radio, portable audio, home stereo, and computers. The ability to design for a wide variety of performance and cost objectives makes such a wide range of applications possible.

In analyzing these applications we have put together a simple Audio System model which we refer to as the Audio Chain. This Chain, as we call it, includes the Amplifier, Control functions such as volume and tone, Converters such as CODEC's, and Digital Signal Processing. Some applications are very simple and may require only the amplifier while others include all aspects of the chain including software.

National began supplying Audio power amplifiers in the 1970's, expanded into Analog Controls in the early 1980's, and has added CODEC's and Digital Acceleration in the 1990's. In the following section you will see how National is providing solutions that address all aspects of the Audio Chain.

The Audio Chain
Progress in providing the "total" solution



More Power

More Channels

New Packaging

National Semiconductor

Analog Solutions 3

If there is a constant in Audio, it is the ever increasing desire for more power. The trend continues in traditional markets like home stereo as well as relatively new markets such as portable computing and celular phones. At the same time the power requirements are increasing, the available supply voltages are kept the same or reduced. This trend has led to some interesting application solutions as we will show.

The popularity of home theater has increased the number of amplifier channels required in a system from 2 in a traditional home stereo to as many as six or more. With so many amplifiers in the system power dissipation and proper thermal design become critical, often limiting system performance.

Physical size constraints, especially in portables, has forced the development of new surface mount packages and new heat sinking techniques.

Many Different Topologies

- Single-Ended Outputs
  - Usually Voltage Limited
  - Most Common Amplifier Topology
- Bridged Outputs
  - Usually Power Dissipation Limited
  - Excellent for systems like TV's, Sub Woofers, and Computers where the speaker is inside the chassis
- Paralleled Outputs
  - Usually only useful for limited supply voltages and lower impedance loads

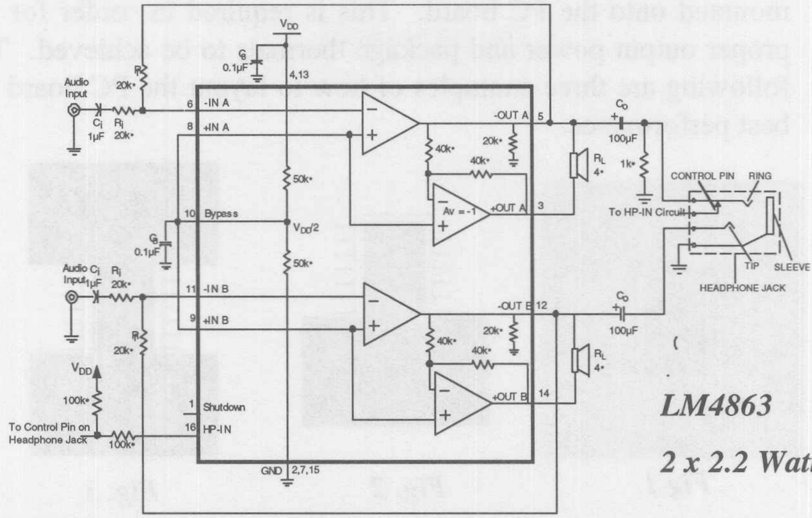
Higher output power can be obtained from many different amplifier topologies. The traditional method is to utilize amplifier ICs in a single ended output configuration. This is what many IC manufacturers strive to provide, however, their fabrication processes tend to be voltage limited.

The most common implementation for voltage limited application is a bridged amplifier configuration. While this method allows a single Dual IC or two Mono ICs to achieve higher output power levels, the downside is the substantial increase in package power dissipation. This solution requires more attention to the thermal design. This type of solution is not limited to self-contained speaker systems but must be used with caution.

A third method of obtaining higher output power levels involves the paralleling of mulitple ICs through ballast resistors to drive higher currents into lower impedance loads. This method solves the IC voltage limitation issue, but places it in a niche for audio applications, as off-the-shelf speakers are generally 4 or 8 ohms.

BOOMER™

The Revolution Continues



LM4863

2 x 2.2 Watts

National Semiconductor

Analog Solutions 5

The LM4860/61 were the original mono BOOMER™ Amplifiers capable of delivering 1 Watt into 8 ohms. Since then, a family of parts have been designed around the original cells of the LM4860/61. Along the way improvements have been made and various functions have been integrated.

In addition, more packages are available. Some of the packages available are TSSOP, MSOP, and SSOP, in addition to the SOIC. Exposed DAP packages are also available to allow greater power dissipation for greater output power.

The LM4863 is a stereo 2.2W power amplifier. It contains improved "click and pop" suppression circuitry and a switchable bridged/single-ended amplifier so that one set of amplifiers can be used for both speakers and headphones.

Extra power can be achieved because the LM4863/73 can drive 4ohm loads with the exposed DAP package (MTE). This exposed DAP package allows the die to be cooled by attaching the package to copper area on the PC board to help dissipate heat This added heat dissipation results in double the output power when compared with the first generation parts.

Exposed DAP Mounting

Any package with an exposed DAP requires the DAP to be mounted onto the PC board. This is required in order for the proper output power and package thermals to be achieved. The following are three examples of how to layout the PC board for best performance.

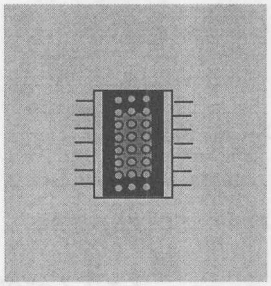


Fig 1.

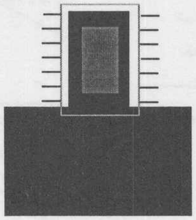


Fig. 2

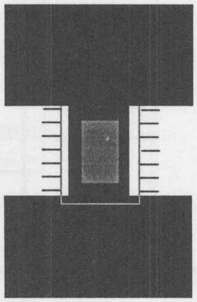


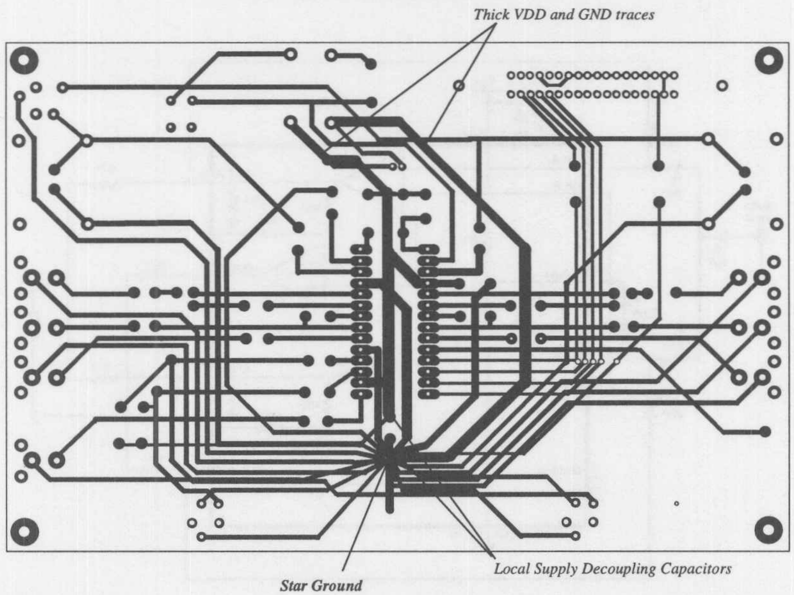
Fig. 3

Figure 1 shows copper on two sides of the PCB. The gray represents the exposed DAP. The black is copper on the top side of the board and the shaded area is copper on the bottom side of the board. The holes are 8 mil vias connecting the top side to the bottom side. It is recommended that 21-30 8 mil vias are placed below the DAP. This allows the heat to flow from the DAP out to the bottom side of the board.

Figure 2 shows black copper on the top side of the PCB. Copper on the top side of the PCB is being used to dissipate the heat coming from the exposed DAP.

Figure 3 is another way of implementing Figure 2. However using a layout similar to the one shown in Figure 3 or any similar “Dog Bone” shape potentially violates U.S. Patent #5,594,234 claim 12. To avoid potential patent infringement, it is recommended to use a layout similar to Figure 2. Test results have shown that the output power is exactly the same for an exposed DAP amplifier mounted in both situations.

Boomer Amplifier Layout

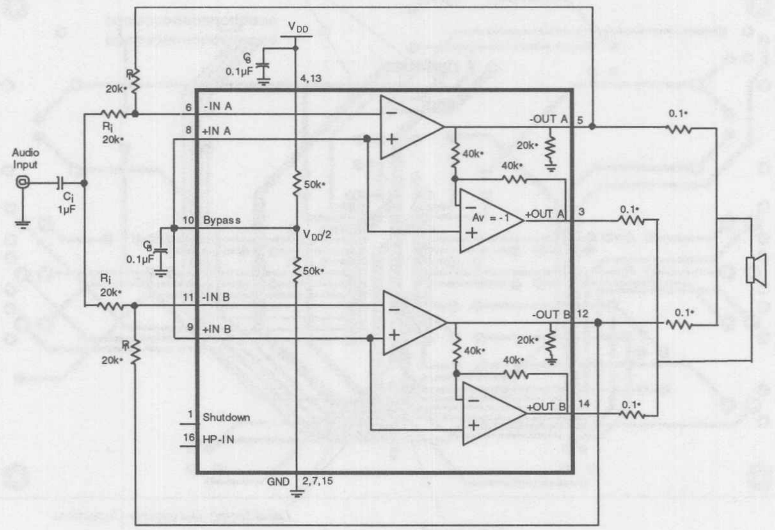


Whenever possible star type ground returns should be used in the PC board layout. This will increase audio performance by reducing THD & noise.

Small local supply decoupling capacitors should be used in parallel with larger supply decoupling capacitor. Typically a 0.1uF capacitor should be placed as close to the IC as possible. Each supply pin should have its own decoupling capacitor.

Use thick (70-100mil) traces for the VDD, GND, and output pins. The larger the trace the smaller the resistance. For low voltage applications it is desired to lose as little potential as possible. This is achieved by using as thick a trace as possible.

Parallel LM4863

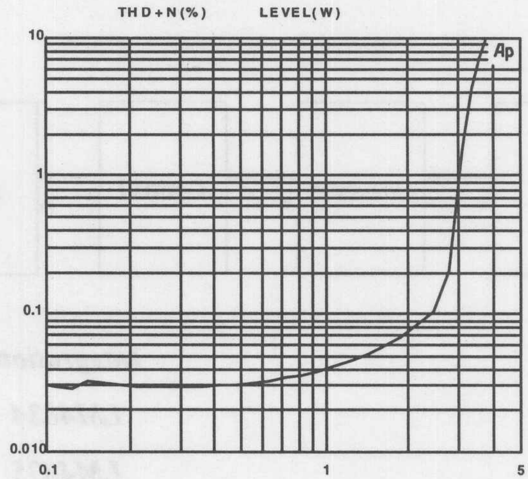


Some Boomer applications require even more output power than before with the same 5V supply voltage. The only way to provide more output power with the same supply is to increase the current drive and reduce the load resistance. Computer manufacturers have started to use 3ohm speakers to attain more output power on 5V.

Shown above is how an LM4863 can be used with the left and right sides paralleled together. By combining the left and right sides we obtain a one channel amplifier with much higher output power. The inputs are also tied together. The outputs are summed together with 0.1ohm resistors.

THD+N vs Power

Parallel LM4863

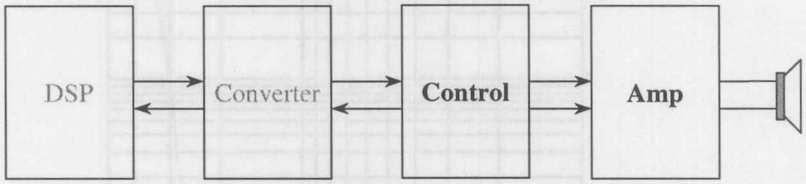


The LM4863 and LM4873 can obtain 3W of output power with a 3ohm load at 1% THD. The biggest trade off in paralleling Boomers is the cost. A designer will need two amplifiers per channel and the summing resistors at the output, which increase the number of external components.

However, paralleling is the only effective way to drive less than 4 ohm load speakers without any large heat sinking or fan cooling.

The Audio Chain

Progress in providing the "total" solution



Integration

LM4834

LM4835

National Semiconductor — Analog Solutions 10

The LM4834 is useful in both desktop and portable PC applications because of its integrated features. It contains: one 1.75W power amplifier, stereo headphone/lineout drivers, a microphone pre-amp with its own power supply, a volume control, and National's "click and pop suppression" circuitry.

The volume control is operated with an external potentiometer that provides a DC potential to the DC volume control input. As the voltage is increased the signal at the outputs is also increased. Various mode controls on the LM4834 allow separate control of the power amp and the headphone amp.

The microphone pre-amp can be used either differentially or single ended. The microphone supply is a power supply buffer for phantom powered microphones.

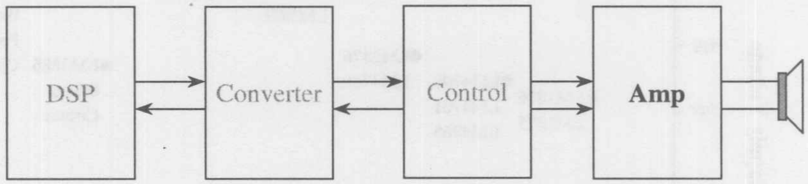
The LM4835 was intended for applications that require stereo speaker and headphone outputs such as portable PCs.

The LM4835 incorporates stereo 2W power amplifiers, stereo headphone/lineout amplifiers, click and pop suppression circuitry and a DC volume control. It also features internal and external selectable gain that can be configured for bass boost. Stereo lineouts are also readily available for connections to docking stations.

All these features make the LM4835 the ideal solution for portable PC audio. The LM4835 as well as all of the Boomer Amplifiers are compliant with Microsoft's PC98/99 specification.

The Audio Chain

Progress in providing the "total" solution



More Power

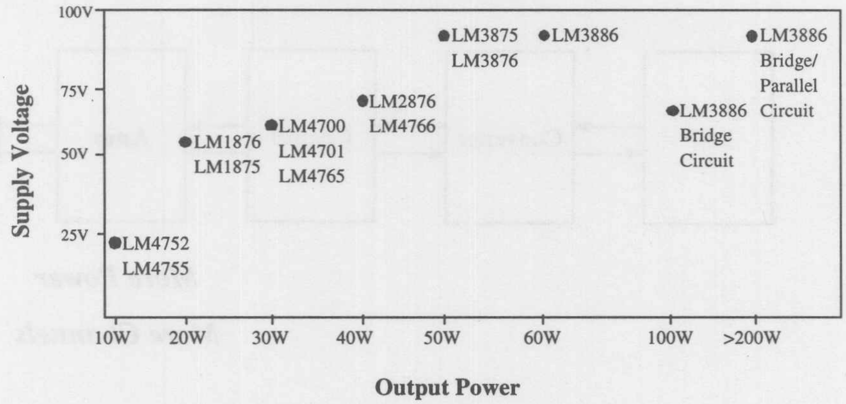
More Channels

National Semiconductor

We have looked at various Boomer solutions including additional applications to increase power with a 5 Volt supply. This, however, only begins to scratch the surface of power amplifier solutions.

National has been in the monolithic amplifier business for over 20 years. Our Overture amplifiers have earned a solid reputation for high power, low THD, excellent sound, and bullet proof protection.

National Has All Power Levels



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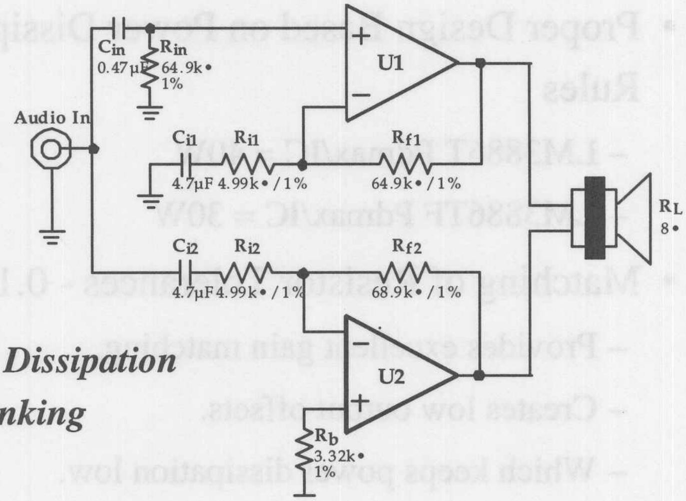
Analog Solutions 12

This figure represents the most recent power amplifiers that National has to offer above the 10W range, including the specialized high power circuits. Notice that there is a solution for practically every power level.

The trend for higher power is everywhere from Laptop & Desktop Computers to TVs & Minicomponent Systems and Home Theater Amplifiers. New applications such as self-powered speakers and subwoofers as well as Dolby™ Digital 5.1 have increased the need for more amplifiers and higher output power. With the development of AC-3 systems, many multichannel amplifiers now provide equal power to all 5 speakers; many at the 100W level.

There are many topologies that can achieve higher power than a single LM3886, but many cannot provide the full SPiKe™ Protection already included in each OVERTURE™ IC, at least without considerable design work. However, there are three circuits that do provide higher power levels while maintaining full protection; a bridged circuit, a paralleled circuit and a bridged/paralleled circuit. One of the main advantages of these solutions are their simplicity of implementation. So, system designers are able to have higher power levels with the highest level of protection and simplicity from these circuits using our power ICs.

Bridge Design Schematics



Power Dissipation

Heatsinking

Using two power ICs in a bridge configuration not only increases the output power by a factor of 4 but also increases the total power dissipation of the solution by a factor of 4, from a single-ended amplifier solution. Therefore, the power dissipation per IC for a 2 IC implementation increases by a factor of 2.

(Single-ended Solution) $\quad Pdmax = Vcc^2/20R_L$

(Bridge Solution) $Pdmax = 4(Vcc^2/20R_L)$

An increased amount of power dissipation per IC places more concern on the heatsinking. Below are a list of important factors used in the determination of the heatsink thermal resistance.

TO-220 Pkg Non-Isolated "T" pkg Thermal Resistance, $\theta_{JC} = 1°C/W$

TO-220 Pkg Isolated "TF" pkg Thermal Resistance, $\theta_{JC} = 2°C/W$

Isolating Washers Thermal Resistance, $0.2°C/W < \theta_{CS} < 1°C/W$

Heatsink Thermal Resistance to be determined, θ_{SA}

$\theta_{SA} = [Tj - Ta - Pdmax(\theta_{JC} + \theta_{CS})] / Pdmax$

Where Tj = 150°C and Ta = 25°C to 50°C

Examples: Pdmax = 40W/IC with 1. Ta = 25°C and 2. Ta = 50°C

1. θ_{SA} = [150°C - 25°C - 40W(1°C/W + 0.5°C/W)] / 40W = 1.6°C/W per IC
2. θ_{SA} = [150°C - 50°C - 40W(1°C/W + 0.5°C/W)] / 40W = 1.0°C/W per IC

Bridge Circuit Critical Design Parameters

- Proper Design Based on Power Dissipation Rules
  - – LM3886T Pdmax/IC = 40W
  - – LM3886TF Pdmax/IC = 30W
- Matching of Resistor Tolerances - 0.1%
  - – Provides excellent gain matching.
  - – Creates low output offsets.
  - – Which keeps power dissipation low.

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Analog Solutions 14

Using the previous page's design equations with the above power dissipation rules for the LM3886T and LM3886TF, a bridge circuit can be designed with any supply voltage with any load AS LONG AS the above power dissipation limitations are not exceeded AND proper heat sinking is utilized.

In addition to the thermal design constraints, the electrical design constraints are limited to the matching of gain and input termination resistor matching. The matching of these resistors is important to keep each IC output close to the other so that no continuous DC current flows through the load. This is bad for two reasons; 1, it increases IC power dissipation, and 2, it extends the cone of the speaker driver in one direction so that it is much easier for AC signals to cause the cone to "bottom out." The DC current through the coil also does not help the long-term reliability of the driver.

A Bridged Solution, BR100

- LM3886T (Pdmax/IC = 40W)
- Vccfl = ±25V, Vccnl = ±32V (max)
  - Transformer Secondaries ±22Vrms (190VA)
- Po = 110W into 8Ω @ onset of clipping
  - Po = 140W @ 10% THD
- THD+N < 0.02% for Po >1W from 20Hz - 20kHz!!

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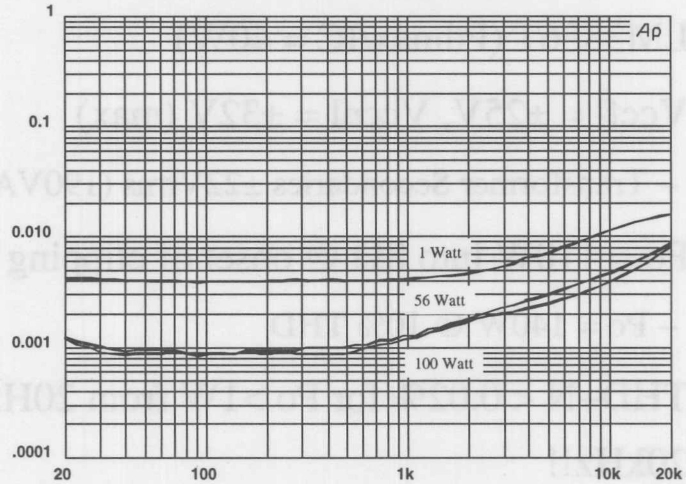
Analog Solutions 15

The bridged solution using the LM3886T was designed with a maximum of 40W of power dissipation per IC and a load of 8 Ω. The supply voltages were calculated to be ±28V, but with unregulated supplies, this voltage was chosen to be approximately the half-way point between the no-load and full-load supply voltages. The no-load supply voltage was chosen to be ±32V while the full-load voltage using a 190VA transformer turned out to be ±25V. These voltages were adequate for attaining 100W into 8 Ω.

BR100 Topology Performance

BR100 THD+N vs Freq Rl=8 ohms Vcc=+/-25.5V BW<80kHz Po=1W, 56W, 100W



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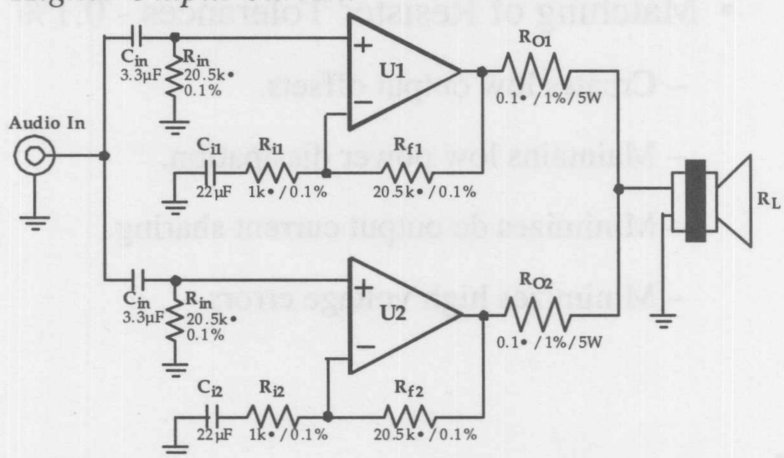
Analog Solutions 16

The excellent performance of a single LM3886 is applied to the bridge circuit as well, resulting in excellent THD+N of 0.02% for all power levels greater than 1W from 20Hz to 20kHz, as shown above. In addition, the high-power linearity is actually much closer to 0.001% THD+N for most of the audio spectrum!

Parallel Design Schematics

Lower Power Dissipation per IC or

Higher Output Current



National Semiconductor — *Analog Solutions* 17

The concept of paralleling amplifiers can provide one of two advantages for a given solution depending upon the application need.

Situation #1: Lower Power Dissipation (Constant Load, Smaller Heatsink)

For a 60W/4 Ω solution, the maximum power dissipation for one LM3886T is about 40W. The power dissipation of this one IC can be decreased by adding a second IC in parallel where each IC now supplies half of the output current. In doing this, each IC's power dissipation is halved (20W), allowing them to run cooler. From a thermal design standpoint, this reduces the heatsinking requirements.

Situation #2: Higher Output Current (Lower Impedance Load, Constant Heatsink)

For a given heatsink size which can dissipate a maximum amount of power, say 40W, the amount of output power is increased based on two ICs instead of one and a lower impedance load. Each IC supplies half of the current to a lower impedance load, providing more output power.

The design concept to keep in mind for paralleling two amplifiers is that each IC sees a load which is twice the acutal load. In essence, each IC is now working half as hard by supplying only half as much output current.

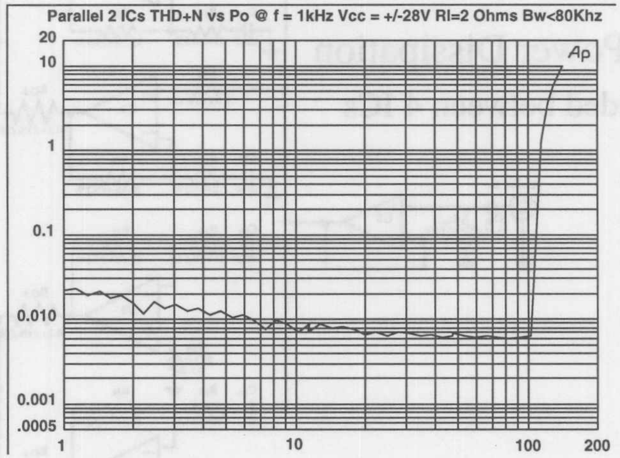
Parallel Circuit Critical Design Parameters

- Matching of Resistor Tolerances - 0.1%
  - Creates low output offsets.
  - Maintains low power dissipation.
  - Minimizes dc output current sharing.
  - Minimizes high voltage errors.

The matching of gain resistors and input termination resistors are required to keep the IC output offsets as low as possible to minimize unnecessary power dissipation. In addition, at high output signal levels, mismatches in amplifier gains can cause subtle offsets in output voltages that may cause one amplifier to drive the other; again increasing power dissipation.

For this design, it IS critical that gain resistor matching be close for proper operation. Looser tolerance resistors will result in larger offsets which will significantly increase IC power dissipation, which negates the concept of reducing IC power dissipation by output current sharing.

Parallel Topology Performance



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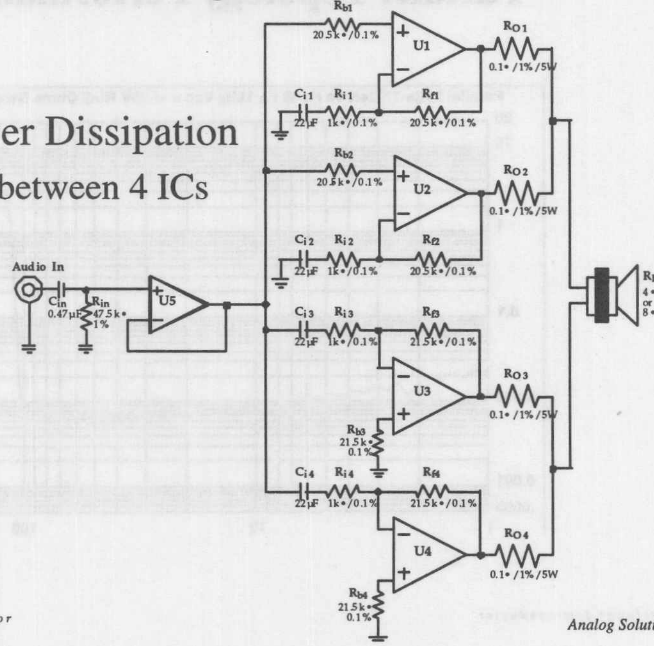
The plot above for the paralleling of two LM3886Ts demonstrates that the power attainable from two ICs driving a 2Ω load with ±28V can reach 100W! This plot backs up the concept of design by power dissipation of the LM3886T where the Pdmax = 40W. Calculating the Pdmax for Vcc = ±28V and with R_L = 2 Ω results in a maximum power dissipation of 78.4W which when divided between the two ICs results in 39.2W per IC.

Remembering that the bridging of two LM3886Ts from Vcc = ±28V while driving an 8 Ω load will result in 100W of output power with 78.4W of total power dissipation. When this total power is divided between the two ICs, each IC power dissipation is 39.2W.

Reaching 100W by driving an 8 Ω load with the bridge circuit is equivalent to reaching 100W by driving 2 Ω with the parallel circuit FROM THE SAME POWER SUPPLY VOLTAGE.

BPA Design Schematics

- Total Power Dissipation
  - Divided between 4 ICs



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Analog Solutions 20

The schematics for the Bridge/Parallel Amplifier (BPA) design is shown above. The topology is essentially a bridged type output with two ICs paralleled on each side of the bridge. One side of the bridge employs non-inverting amplifiers while the opposite side employs inverting amplifiers. There is an op amp used as a buffer to minimize the differences in input impedance between the non-inverting and inverting amplifier stages. Low impedance, high power ballast resistors are used to tie each output together before driving the load.

(Bridge Solution) $Pdmax = 4(Vcc^2/20R_L)$

Divide BRidge Solution Pdmax by Number of ICs in Parallel

(BPA Solution) $Pdmax = 4(Vcc^2/20R_L) / n$ (where n = 4 ICs)

$$Pdmax = Vcc^2/20R_L$$

An increased amount of power dissipation per IC places more concern on the heatsinking. Below are a list of important factors used in the determination of the heatsink thermal resistance.

TO-220 Pkg Non-Isolated "T" pkg Thermal Resistance, $\theta_{JC} = 1°C/W$

TO-220 Pkg Non-Isolated "TF" pkg Thermal Resistance, $\theta_{JC} = 2°C/W$

Isolating Washers $0.2°C/W < \theta_{CS} < 1°C/W$

Heatsink Thermal Resistance to be determined, θ_{SA}

$\theta_{SA} = [Tj - Ta - Pdmax(\theta_{JC} + \theta_{CS})] / Pdmax$ (where Tj = 150°C and Ta = 25°C to 50°C)

Examples: Pdmax = 40W/IC with 1. Ta = 25°C and 2. Ta = 50°C

1. θ_{SA} = [150°C - 25°C - 40W(1°C/W + 0.5°C/W)] / 40W = 1.6°C/W per IC
2. θ_{SA} = [150°C - 50°C - 40W(1°C/W + 0.5°C/W)] / 40W = 1.0°C/W per IC

BPA Critical Design Parameters

- Design Based on Power Dissipation
  - LM3886T Pdmax/IC = 40W
  - LM3886TF Pdmax/IC = 30W
- Matching of Resistor Tolerances - 0.1%
  - Creates low output offsets.
  - Creates low power dissipation.
  - Minimizes dc output current sharing.
  - Minimizes high voltage errors.
- Input Buffer for Input Impedance Differences

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Analog Solutions 21

The key design parameters for the bridge/parallel amplifier are the maximum power dissipation per IC, the matching of gain and offset resistor tolerances.

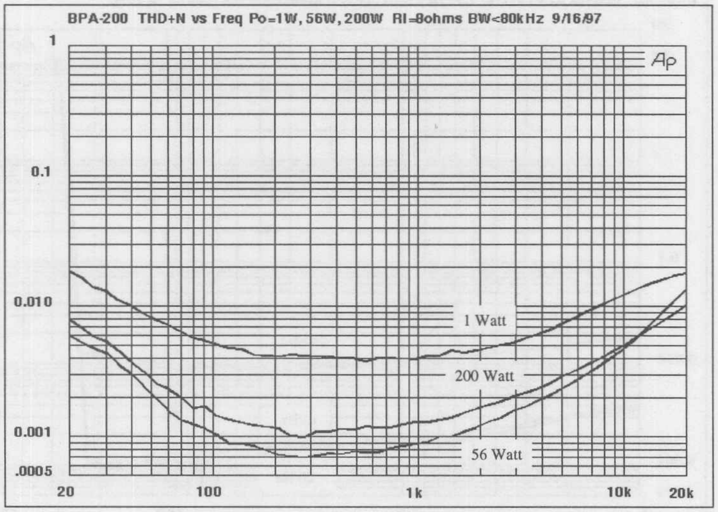
The bridge/parallel design topology is based solely on power dissipation capabilities. The bridging of two ICs increases the total power dissipation by a factor of 4 as stated previously, so the power dissipation for each IC would be doubled. The paralleling of two ICs divides the solution power dissipation between each IC. When combining two paralleled devices with two more paralleled devices in a bridged type configuration the power dissipation for each IC is the same as a normal single-ended amplifier configuration.

The matching of gain resistors and input termination resistors are required to keep the IC output offsets as low as possible to minimize unnecessary power dissipation. In addition, at high output signal levels, mismatches in amplifier gains can cause subtle offsets in output voltages that may cause one amplifier to drive the other; again increasing power dissipation.

A Bridged/Paralleled Solution

- **LM3886T (Pdmax/IC= 40W)**
  - 2 ICs per Bridge Output are Paralleled
- **Vccfl = ±35V, Vccnl = ±42V (max)**
  - Transformer Secondaries ±30Vrms (385VA)
- **Po = 225W into 8 Ω** @ onset of clipping
  - Po = 295W Burst Clipping Point Power (f=20Hz)
- **Po = 335W into 4 Ω** @ onset of clipping
  - Po = 450W Burst Clipping Point Power (f=20Hz)
- **THD+N<0.02%**, Po>1W from 20Hz-20kHz!!

BPA THD vs Frequency Performance



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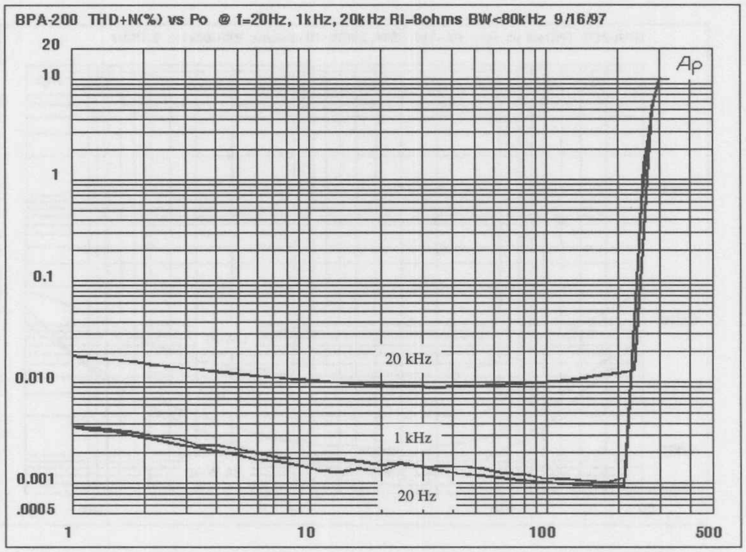
Analog Solutions 23

As can be seen by the THD vs Frequency plot for Po = 1W, 56W and 200W, the THD is less than 0.02% for all frequencies and for all power levels greater than 1W into an 8 Ω load.

Notice that for midband frequencies and higher power levels the THD is around 0.001% or less.

BPA THD vs Output Power Performance



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Analog Solutions 24

The THD vs Output Power plot for 20Hz, 1kHz, and 20kHz frequencies show above, demonstrates the excellent performance of the Bridge/Parallel design.

The highest THD curve is for the 20kHz frequency, but is relatively flat for all power levels at around 0.01% THD. For lower frequencies (20Hz to 1kHz) the THD is more around the 0.001% THD level.

Notice that the clipping point powers are around the 225W range for the ±35V full-load supplies.

Parallel More Devices

- By Paralleling More Devices,
  - IC Power Dissipation can be further reduced,
  - allowing lower impedance loads to be driven,
  - achieving even Higher Power Levels!
- Try 3 or 4 ICs per side for
  - Bridged/Paralleled Output!!

National Semiconductor

Analog Solutions 25

One major benefit of the Bridge/Parallel design is that more devices can be paralleled per bridge side to further reduce the IC power dissipation or drive a lower impedance load.

There is a limit to how much you can reduce the power dissipation by paralleling more devices, and it depends a lot on how much power is required to be delivered to the load and how low of a load impedance is to be driven. One ohm loads and less can be driven successfully if proper thermal design techniques are employed. Adding 5 or more devices in parallel per bridge side to drive either a 4 Ω or 8 Ω load is not practical. 4 devices in parallel to drive a 4 Ω load at high supply voltages seems to be adequate.

Amplifier Applications

- Bridge Circuit
  - Computer Subwoofers
  - Home Theater Subwoofers
  - Self-Powered Speakers
- Parallel Circuit
  - High-Power, Low Impedance Solutions
  - High-Power, Low Voltage Supply Requirements
- Bridge/Parallel Circuit
  - Home Entertainment Amplifiers
  - Self-Powered Speakers and AC-3 Subwoofers

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Analog Solutions 26

The Bridge Circuit is a simple way to achieve excellent performance and high power with full protection for 100W applications like self-powered speakers and subwoofers.

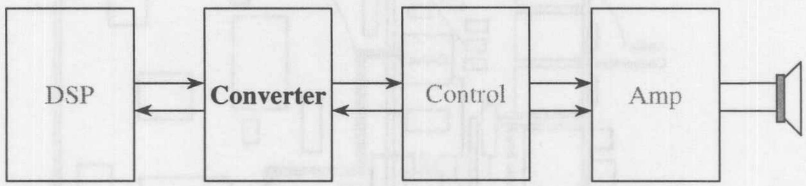
The Parallel Circuit is a great way to achieve higher power when constrained by low voltage supplies, by driving low impedance loads.

While many integrated amplifiers or receivers on the market are of the "single-ended" topology, there are some manufacturers that have implemented the BPA design for high-end multichannel home theater amplifiers. Customers tend to like the simple design with the exceptional performance and the added protection that these parts offer. Many customers have already implemented the topology for self-powered speakers and subwoofers. This topology is useful towards any really high power solution where simplicity and full protection are needed.

Finally, National has a full line of power amplifiers and solutions to meet the needs of practically every power level.

The Audio Chain

Progress in providing the "total" solution

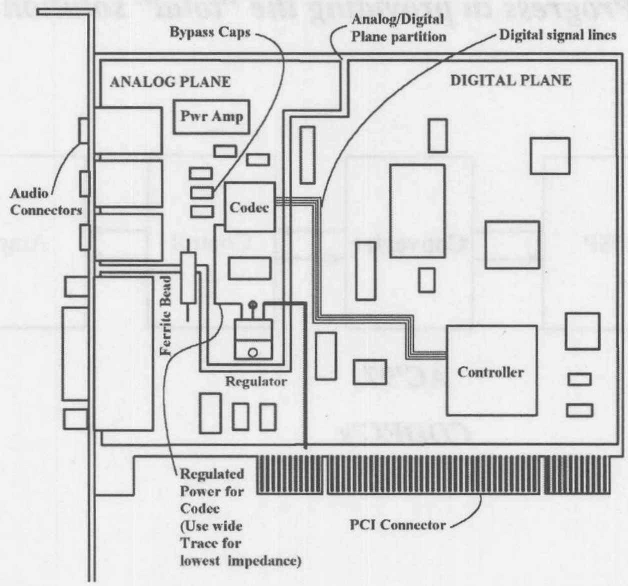


AC'97

CODEC's

CODECs represent National's first entry into Digital Audio. This effort began with the introduction of the LM454 and now includes a growing family of AC'97 six devices for the PC market.

Codec Layout Guidelines



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Analog Solutions 28

The PCB layout for a CODEC on a mixed signal board, such as a sound card or mother board, is critical for optimum performance. In order to avoid a poor noise floor or tones present in the output a few layout ground rules should be followed. For this discussion, a PCI sound card will be shown as an example. Figure 1 illustrates a typical sound card.

Poor layouts often have the following problems:

1) No ground plane to minimize unwanted radiation of fast digital transitions.

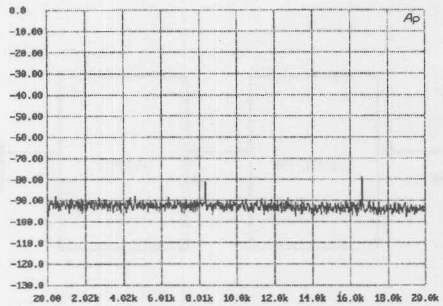
2) No ground plane partitioning such that digital noise degrades analog performance.

3) Supply bypassing is not carefully thought out.

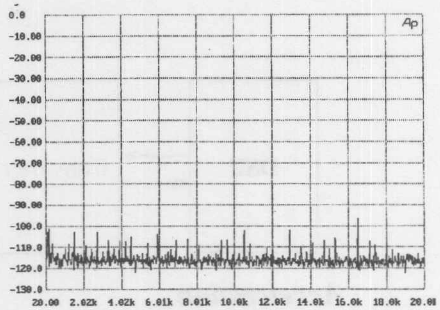
4) No analog supply regulation is included for noise rejection from the PC's power supply.

5) Digital signals pass over analog signals or analog ground planes.

CODEC S/N vs Layout



Graph 1



Graph 2

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Analog Solutions 29

The first graph shows the DAC noise level (relative to full scale output) and tones present from a poor layout. The second graph shows reduction in noise after several improvements were made

1) Partitioned analog and digital ground planes.

2) Analog and digital ground planes have a wide isolation margin and do not overlap. (2mm is good)

3) Suppy and Vref by-passing is placed as close as possible to the CODEC pins

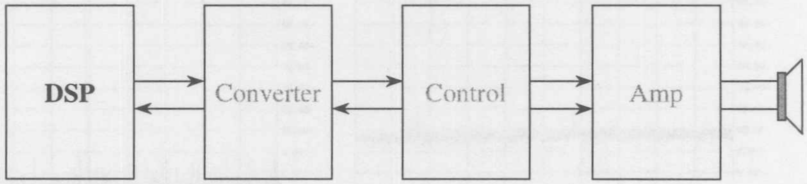
4) Voltage regulation is provided with good by-passing and with judicious placement of the regulator.

5) Analog and digital ground planes connect at a single point with a ferrite bead to isolate switching transients from the quiet analog ground.

6) Digital signals are routed only over digital ground and analog signals only over analog ground.

The Audio Chain

Progress in providing the "total" solution



Acceleration

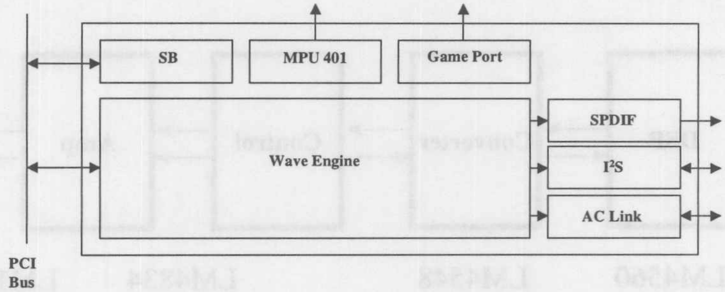
Legacy

National Semiconductor

Analog Solutions 30

National Audio has entered the DSP market with the introduction of its DC'97 compliant PCI Digital Audio Accelerator. The LM4560 provides significant system level performance enhancement over an equivalent ISA Audio Controller.

LM4560 PCI Audio Accelerator

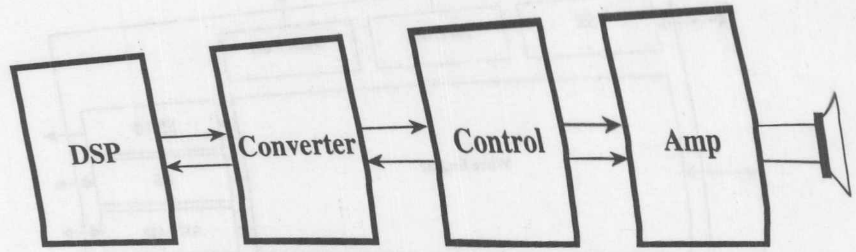


- Reduces CPU overhead as much as 8 to 1
- 64 Audio channels
- Supports AC'97 Rev 2.1
- Supports I^{2}S, S/P DIF, DLS1
- Full legacy compatibility
- 3.3 volt operation
- 100 pin TQFP package

When used with an AC'97 CODEC and optional audio amplifier, the LM4560 will provide a complete PCI audio solution for sound cards, desktops, and laptop computers. The high performance hardware acceleration significantly reduces the CPU overhead associated with Audio support thus freeing resources for other tasks. This is critical when applied to PC games or concurrent applications.

Product Summary

Providing the "total" solution



DSP	Converter	Control	Amp
LM4560	LM4548	LM4834	LM1876
	LM4547	LM4835	LM2876
	LM4546	LM4873	LM3876
	LM4545	LM4880	LM3886
	LM4543	LM4881	LM4701
	LM4540	LM4882	LM4752
			LM4755

National Semiconductor

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As we have shown, National is now capable providing Audio solutions for the entire Audio Chain. We started with Analog power amplifiers, added controls, developed a full line of AC'97 CODEC's, and just introduced our first DSP solution.